Fermilab

RF Note #076

The Mid-Level RF (MRF) Handbook

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Abstract: The intent of this handbook is to document, at least to first order, the design and features of the Mid-Level RF (MRF) system. During the MRF development, the relationship between many already existing parameters and new parameters had to be deeply understood and would have benefited from a document such as this. It can be read from start to finish or as a handbook using the table of contents below.

Amplitude Regulation System

There are three amplitude loops that are responsible for regulating the MI h588 system cavity voltage. Listed in order of innermost loop to outermost loop, they are:

- Direct RF FB Loop
- Screen Current Regulation Loop
- MRF Amplitude Regulation Loop

The RF feed-forward beam loading compensation system is not considered here since it is not directly applicable to this discussion.

This discussion reviews the design equations used to minimize the control effort of each of the above loops in steady-state. The equations presented here are simple static gain equations that define how all the pieces of the system are related and fit together as a whole. The simplified block diagram model of the entire MI h588 vector control system as shown in Figure 1 on the following page is used to define the design equations.

Direct RF FB Loop Steady-State Design Equations

There are essentially three concerns for this discussion of the Direct RF FB loop:

- Providing the proper RF drive signal to the station in order to produce the requested cavity gap voltage. This leads to the 'open loop design equation' which is discussed below.
- Satisfying the 'Direct RF FB zero error condition' which simply means that the error between the requested cavity gap voltage and the actual cavity gap voltage should be reduced to zero.
- Providing an adequate range in Direct RF FB gain.

➢ *Open Loop Design Equation*

To understand the proper RF drive levels necessary to drive a HLRF station, the 'open loop design equation' is used:

Open Loop Design Equation: $v_{Gap} = v_{Drive} \cdot G_{OLG} G_{Sys}$

v_{Gap} : the station cavity gap voltage

v_{Drive} : the RF drive level inside the Station RF Controller immediately before its 'drive + error' summing junction (at J3 of its schematic)

G_{OLG} : the internal variable gain of the Station RF Controller between v_{Drive} and the Station RF Controller's output immediately before its final 8-way splitter, v_{SSD} (at the output of U14 of its schematic)

G_{Sys} : the gain of a HLRF station system between v_{SSD} and the station's cavity gap voltage.

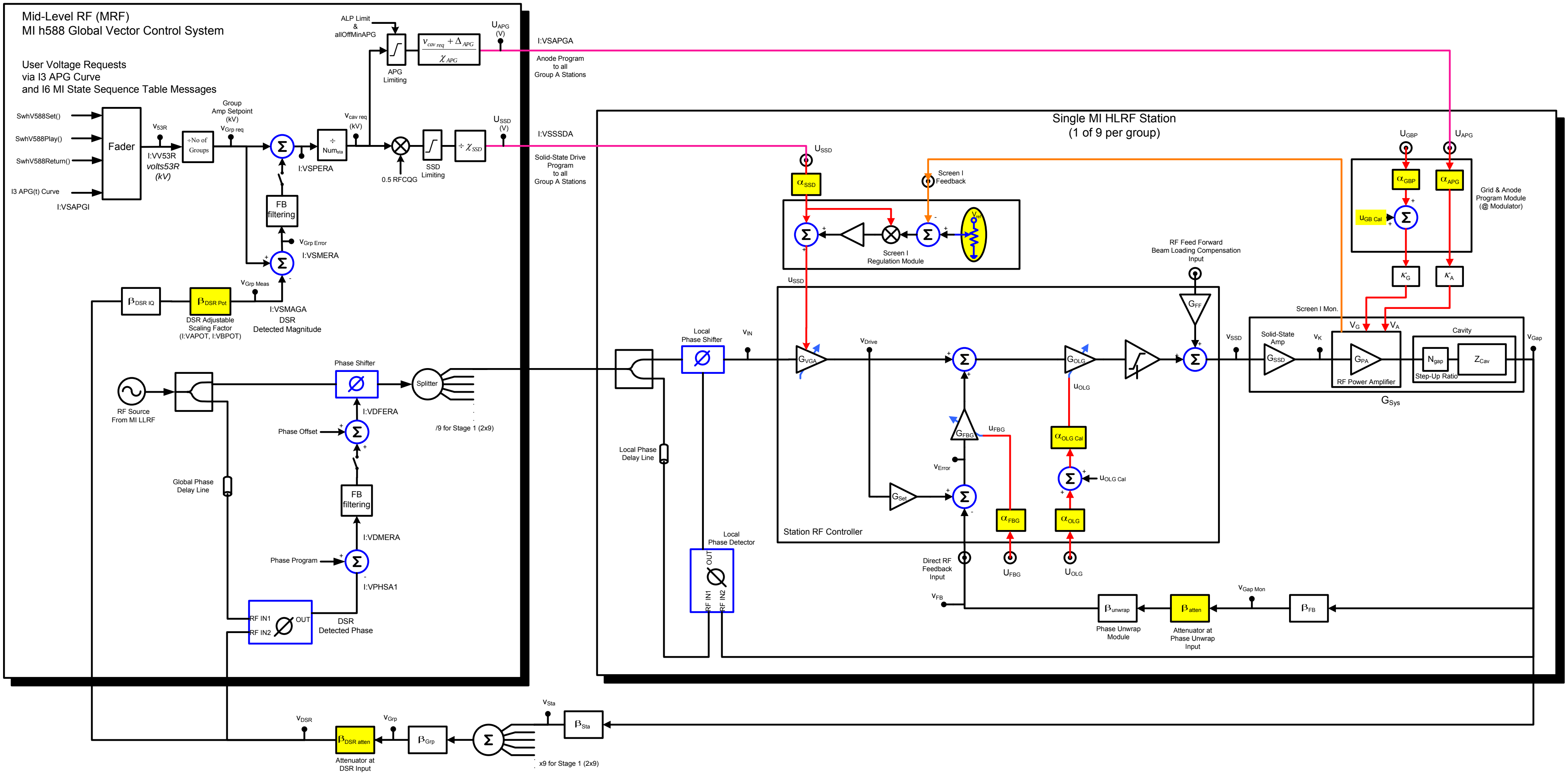


Figure 1: Block diagram of the MRF system including a typical HLRF station.

G_{Sys} lumps together the gain through the Station RF Controller's 8-way splitter, the SSD amplifiers, the 8-way combiner, the PA cathode circuit, and the PA tube in conjunction with the cavity impedance and cavity gap to anode step-up ratio. It is a complicated function of PA anode bias, PA grid bias, RF drive level, frequency, cavity step-up ratio, and cavity impedance. For an understanding of its range, see Ref. [2].

The purpose of G_{OLG} being a variable gain term is to dynamically compensate for predictable changes in G_{Sys} in order to keep the product $G_{OLG}G_{Sys}$ constant. Keeping this product constant not only maintains a constant proportionality between v_{Gap} and v_{Drive}, it also maintains a constant Direct RF FB loop gain. The station gain is an increasing function of frequency, anode bias, and grid bias. In fact the station gain can change by as much as 17dB over the operating parameter space (see Ref [2]). Maintaining a constant Direct RF FB loop gain would ensure that the stability margin is also maintained at all points of operation; thus no one point of operation limits the gain for the other points of operation. Currently beam loading compensation is crucial at injection for slip-stacking whose operating point is near the lowest system gain. For a detailed discussion of the design of G_{OLG} see the section entitled "The Open Loop Gain Compensation (RFOLG) Function".

The nominal design values for both G_{Sys} and G_{OLG} were determined based upon many practical considerations including:

- The range in G_{Sys} over the practical operating parameter space
- PA tube aging, which can cause a gain reduction as much as ~2dB
- Station to station system gain variations including cavity step-up ratio variations
- Measurements of Station RF Controller module-to-module gain variations

See 'The Variable Gain Amplifier' section (p.24) for the actual design nominal values.

➤ *Direct RF FB Zero Error Condition*

To minimize the control effort of the Direct RF FB loop, the open loop response should ideally produce zero error when there are no perturbations to the nominal system gain. In order to nominally have $v_{Error} = 0$ in open loop, the following equation must be satisfied:

Direct RF FB Zero Error Condition: $v_{Drive} \cdot G_{Set} = v_{FB}$

where $v_{FB} = v_{Gap} \cdot \beta_{FB}\, \beta_{atten}\, \beta_{unwrap}$

v_{FB} : the Direct RF FB signal supplied to the Station RF Controller. It is a scaled version of the cavity gap voltage.

G_{Set} : an internal Station RF Controller gain on v_{Drive} whose value was designed to satisfy the Direct RF FB zero error condition for the nominal gain of all loop components.

β_{FB} : the cavity gap monitor total scaling factor. It includes the upstream cavity gap monitor, the cabling from the cavity to the station equipment racks, and the splitter and cabling inside the station equipment rack to the "upstream gap monitor" which is used as the Direct RF FB signal

β_{atten} : the scaling associated with the attenuator used at the input to the phase unwrap module. It is tuned during station calibrations to satisfy the zero error condition at the calibration point.

β_{unwrap} : the nominal gain of the phase unwrap module.

The Direct RF FB zero error condition has to be satisfied in both magnitude and phase. In practice the phase is usually matched first by adjusting the phase unwrap delay line until the magnitude of v_{Error} is minimized. Then the magnitude is matched using a combination of β_{atten}, G_{OLG}, and v_{Drive}. The purpose of the phase unwrap module is to 'unwrap' the natural phase slope across the 300kHz frequency sweep that occurs due to the HLRF station's physical loop delay, essentially from v_{Drive} to v_{FB}.

- ***The Direct RF FB Gain (RFFBG)***

Due to the 'drive+error' design of the Station RF Controller, the Direct RF FB loop gain can be turned on and off using the variable gain G_{FBG}. The beauty of the 'drive+error' design is that it conveniently allows for a calibration to achieve a zero v_{Error} in open loop ($G_{FBG} = 0$).

This 'drive+error' architecture also allows the Direct RF FB gain to be varied without affecting the nominal transfer function gain. The transfer function of the entire direct RF FB loop can be expressed as:

$$\frac{v_{Gap}}{v_{Drive}} = G_{OLG} G_{Sys} \frac{(1 + G_{Set} G_{FBG})}{(1 + \beta_{FB} \beta_{atten} \beta_{unwrap} G_{OLG} G_{Sys} G_{FBG})}$$

From the previous section's discussion β_{atten} is tuned to satisfy the zero error condition. This means that β_{atten} is chosen such that, nominally,

$$\beta_{FB} \beta_{atten} \beta_{unwrap} = \frac{G_{Set}}{G_{OLG\,nom} G_{Sys\,nom}} .$$

where $G_{OLG\,nom}$ and $G_{Sys\,nom}$ indicate the nominal G_{OLG} and G_{Sys} values respectively. This reduces the transfer function to the following:

$$\frac{v_{Gap}}{v_{Drive}} = G_{OLG}G_{Sys}\frac{(1+G_{Set}G_{FBG})}{\left(1+\frac{G_{OLG}G_{Sys}}{G_{OLG\,nom}G_{Sys\,nom}}G_{Set}G_{FBG}\right)}.$$

At the calibration point, G_{OLG} and G_{Sys} are at their nominal values; thus the above reduces to $G_{OLG\,nom}G_{Sys\,nom}$. Away from the calibration point, the ideal purpose of varying G_{OLG} is to keep $G_{OLG}G_{Sys} = G_{OLG\,nom}G_{Sys\,nom}$. Again under this scenario, the above transfer function reduces to $G_{OLG\,nom}G_{Sys\,nom}$. Finally, even if this ideal purpose is not served and there are perturbations in the system gain, it is the job of the Direct RF FB loop itself to reduce the cavity voltage error to zero. In the limit of large Direct RF FB gain, G_{FBG},

$$\lim_{G_{FBG}\to\infty}\frac{v_{Gap}}{v_{Drive}} = G_{OLG\,nom}G_{Sys\,nom} \quad .$$

The Direct RF FB loop gain is the gain around the entire loop. Again, assuming that β_{atten} was calibrated as discussed above, the Direct RF FB Loop Gain equation reduces to:

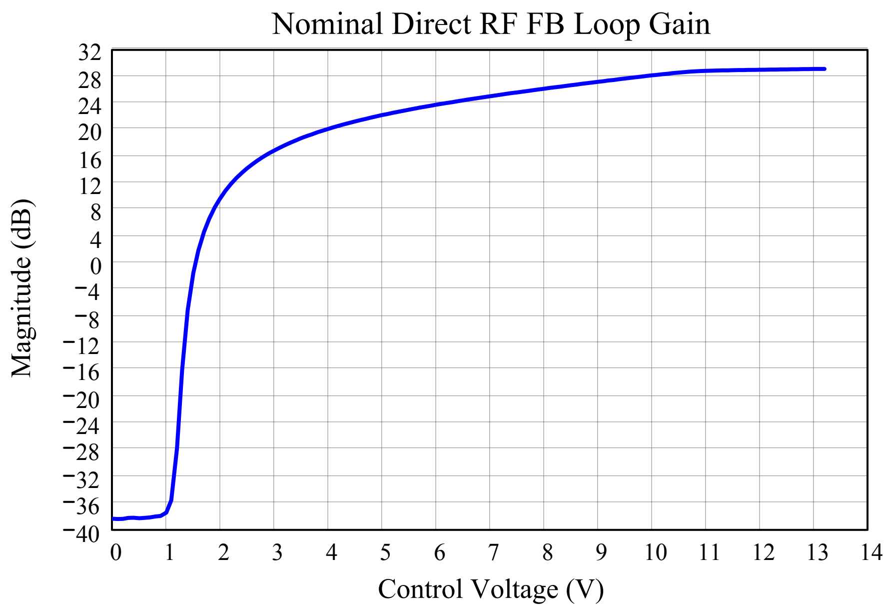
$$\text{Direct RF FB Loop Gain} = G_{Set}G_{FBG}\cdot\frac{G_{OLG}G_{Sys}}{G_{OLG\,nom}G_{Sys\,nom}}$$

This clearly reveals that if the ideal purpose of G_{OLG} is served, then the Direct RF FB Loop Gain is reduced to $G_{Set}G_{FBG}$. The purpose of G_{Set} is now clear. It essentially serves two functions: (1) it matches the drive term to the practical cavity gap voltage monitor signal level that is available, and (2) in combination with G_{FBG} it defines the maximum Direct RF FB loop gain. G_{Set} is realized with an amplifier whose gain is 8.3dB, which corresponds to a linear value for G_{Set} of 2.6 V/V.

The variation in loop gain is obtained via the variable gain G_{FBG}. It is realized in the Station RF Controller via a voltage variable attenuator followed by an amplifier. The voltage variable attenuator is a Mini-Circuits RVA-2500 whose range spans ~ 66dB from –70dB to –4dB. The gain of the amplifier is ~ 28dB. Taking into account a two-way combiner and insertion loss in the Station RF Controller, the range in G_{FBG} is –46dB to +20dB. Combined with G_{Set}, the range in the Direct RF FB loop gain is approximately –37.7dB to +28.3dB, corresponding to a linear range of approximately 0.013 V/V to 26 V/V. Peak drive power during turn on transients of the Direct RF FB loop can be controlled via the ‘Drive+Error Limiter’ in the Station RF Controller.

The control of G_{FBG} is realized via the analog control signal u_{FBG} which is a single HLRF station scaled version (via α_{FBG}) of the global control U_{FBG}. The purpose of α_{FBG} is to provide an individual adjustment at each HLRF station.

Assuming that the Direct RF FB Loop Gain can be expressed as $G_{FBG}G_{Set}$ as discussed above, the nominal Direct RF FB Loop Gain as a function of u_{FBG} is shown on both a logarithmic and linear scale in Fig. 2 below.



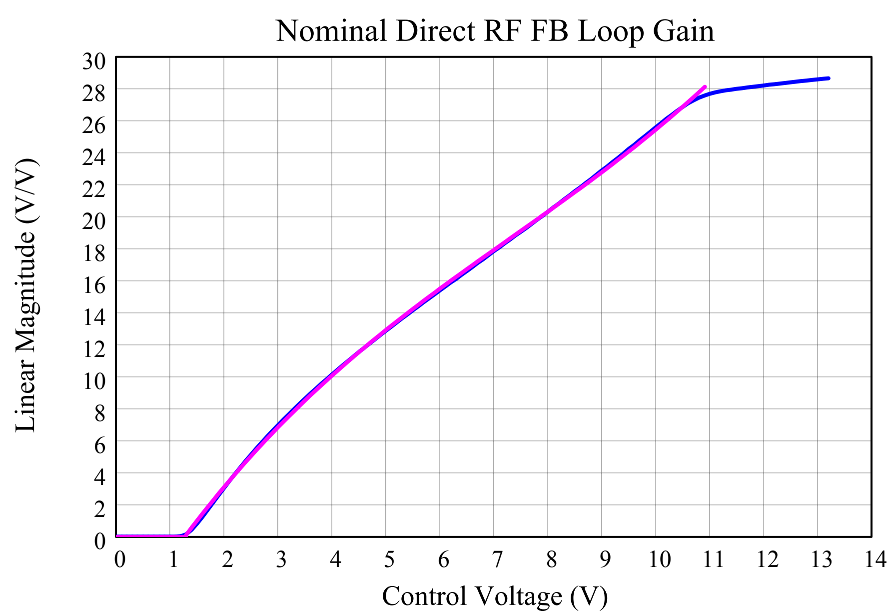


Figure 2: The nominal Direct RF FB Loop Gain as a function of u_{FBG} in dB (top) and linear magnitude (bottom: actual=blue, common transform curve fit=magenta)

The plots in Fig. 2 were generated by combining the measured response of the RVA-2500 with the nominal gain of G_{Set} and the Station RF Controller components which make up G_{FBG} as described above.

The linear magnitude can be approximated by a piecewise continuous function as:

$$Direct\ RF\ FB\ Loop\ Gain\ (u)\ \text{[V/V]}\ =$$

$$0 \quad for \quad u < 1.2724$$

$$0.0193 \cdot u^3 - 0.4242 \cdot u^2 + 5.4911 \cdot u - 6.34 \quad for \quad u \geq 1.2724$$

This form is available via ACNET common transform number 30. Transform 30, with the above coefficients, has been applied to all ACNET devices associated with RFFBG. The primary units of these devices are in Volts, which are the raw I3 units and the raw output units of the CAMAC C465 cards and the MRF DAC Line Driver. Thus on I3 the RFFBG curve, represented in this documentation as U_{FBG}, is tuned in raw units of Volts. To see the actual nominal Direct RF FB Loop Gain (assuming nominally that $\alpha_{FBG} = 1$ such that $u_{FBG} = U_{FBG}$), a fast time plot (FTP) can be used showing the 'engineering units' which are the result of the common transform shown above. The engineering units have been labeled as the dimensionless units of [V/V] to distinguish it as a linear scale. It is important to note the phase response of the RVA-2500 as shown in Fig. 3 when programming the RFFBG curve. It should not be tuned to where the phase response is changing rapidly since the Direct RF FB loop is calibrated with RFFBG ≥ 2 Volts. Of course, it can be tuned to 0 to effectively disable Direct RF FB.

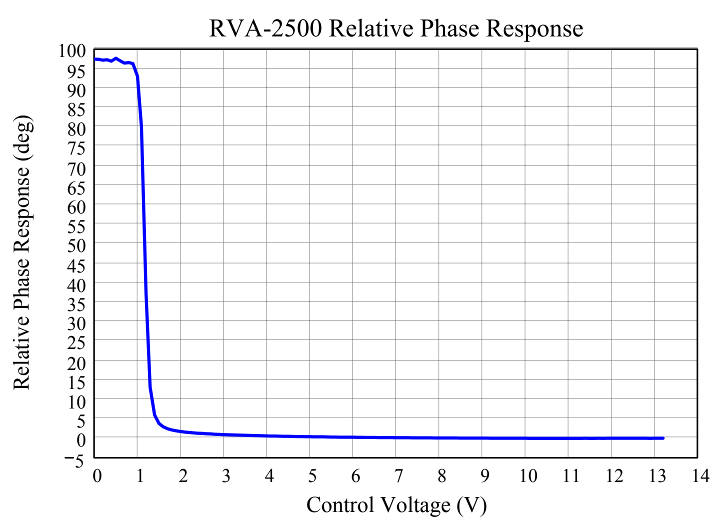


Figure 3: The typical phase response of an RVA-2500.

➢ *The Open Loop Gain Compensation (RFOLG) Function*

The purpose of G_{OLG} has been described in the previous sections as a means to dynamically compensate for predictable changes in the overall system gain G_{Sys}. This section describes the details of the 'Open Loop Gain Compensation' (RFOLG) function design in order that its implementation is properly understood and used.

Figure 4 depicts how the control of G_{OLG} is accomplished.

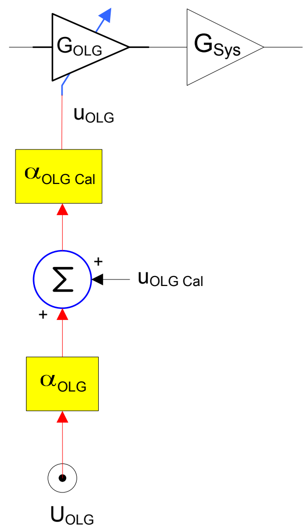


Figure 4: The structure of the RFOLG control

A global RFOLG control signal, U_{OLG}, is sent to all stations. There are two adjustment potentiometers located on the front panel of the Station RF Controller module at each station. One of these potentiometers controls α_{OLG} which is a local station scaling of U_{OLG}. The second potentiometer controls $\alpha_{OLG\,Cal}$ which is a scaling factor for both $\alpha_{OLG}U_{OLG}$ and the internal fixed offset $u_{OLG\,Cal}$. The control signal that is actually delivered to the variable gain amplifier, represented as G_{OLG}, is denoted as u_{OLG} which is considered the local station RFOLG control signal.

This structure has been designed with the intent of U_{OLG} being a bi-polar signal and equal to zero at the calibration point. An individual station's gain at the calibration point is adjusted using $\alpha_{OLG\,Cal}$. For operating points different from the calibration point, U_{OLG} is then programmed to a nonzero value in an attempt to make the station gain equal to the gain at the calibration point. By adjusting α_{OLG}, which applies a scaling to U_{OLG}, the variation in the way each station's gain changes away from the calibration point can be compensated for to first order. Thus, the purpose of these controls and their arrangement is to provide a first order means to calibrate individual stations to an average response. This is further understood through a mathematical description:

- Assume that an individual HLRF station's gain G_{Sys} is a function of frequency, f, and RF power amplifier (PA) tube biasing, V_{bias}. Using a subscript of N to denote a particular station, an individual station's gain can be written as $G_{Sys\,N}\left(f,V_{bias}\right)$.
- Furthermore, assume that the variable gain amplifier, G_{OLG}, has a strictly linear response to the control signal u_{OLG} such that $G_{OLG} = m \cdot u_{OLG}$.

Then a particular station's 'compensated' open loop gain, designated as $G_{OLG}G_{Sys}$, can be written as:

$$G_{OLG}G_{Sys} = m \cdot G_{Sys\,N}\left(f,V_{bias}\right) \cdot \alpha_{OLG\,Cal}\left[u_{OLG\,Cal} + \alpha_{OLG} \cdot U_{OLG}\right]$$

Now let us assume that all the stations will be calibrated under the same conditions; i.e. the same PA tube anode and grid bias, the same RF drive level, and at the same RF frequency. At this 'calibration point' each station will have a system gain denoted as $\left.G_{Sys\,N}\left(f,V_{bias}\right)\right|_{Cal}$; however, we can define a compensated open loop gain, $G_{OLG\,nom}G_{Sys\,nom}$, as the gain which we would like each station to have at the calibration point. The difference between an individual station's gain and the ideal gain can be due to any component in the chain: i.e. the SSD amplifiers, the combiner, the PA tube, the cavity step-up ratio, the components in the Station RF Controller, and even the variable gain amplifier G_{OLG} itself. At the calibration point $U_{OLG} = 0$ by design and we find that the ideal value of $\alpha_{OLG\,Cal}$ will be:

$$\alpha_{OLG\,Cal} = \frac{G_{OLG\,nom}G_{Sys\,nom}}{\left.G_{Sys\,N}\left(f,V_{bias}\right)\right|_{Cal}} \cdot \frac{1}{m \cdot u_{OLG\,Cal}} \quad .$$

Under this condition, the compensated open loop gain becomes:

$$G_{OLG}G_{Sys} = G_{OLG\,nom}G_{Sys\,nom} \cdot \frac{G_{Sys\,N}\left(f,V_{bias}\right)}{\left.G_{Sys\,N}\left(f,V_{bias}\right)\right|_{Cal}} \cdot \left[1 + \frac{\alpha_{OLG}}{u_{OLG\,Cal}} \cdot U_{OLG}\right]$$

We can now begin to define what the ideal U_{OLG} program should be. Assume that at all other operating conditions or points, $\left(f,V_{bias}\right)$, we want to keep the compensated gain, $G_{OLG}G_{Sys}$, constant and equal to the ideal gain, $G_{OLG\,nom}G_{Sys\,nom}$. Thus, to achieve this we must satisfy,

$$1 + \frac{\alpha_{OLG}}{u_{OLG\,Cal}} \cdot U_{OLG} = \frac{\left.G_{Sys\,N}\left(f,V_{bias}\right)\right|_{Cal}}{G_{Sys\,N}\left(f,V_{bias}\right)}$$

This implies that U_{OLG} must become a function of the operating point, $\left(f, V_{bias}\right)$. It can be solved for each station. However, in order not to have 18 separate control signals, we choose to send only one global program to all stations. Thus, we need to determine a single function that is useful for all stations. Let's assume that we can describe an average behavior of all the stations, denoted as $\overline{G_{Sys}}_{Avg}\left(f, V_{bias}\right)$, over all the operating points:

$$\overline{G_{Sys}}_{Avg}\left(f, V_{bias}\right) = \frac{1}{\#\ of\ Stations} \sum_{N=1}^{\#\ of\ Stations} G_{Sys\,N}\left(f, V_{bias}\right) \ .$$

If we define $\alpha_{OLG} = 1$ when a station's gain function equals the average response, then

$$U_{OLG}\left(f, V_{bias}\right) = u_{OLG\,Cal} \cdot \left[\frac{\overline{G_{Sys}}_{Avg}\left(f, V_{bias}\right)\Big|_{Cal}}{\overline{G_{Sys}}_{Avg}\left(f, V_{bias}\right)} - 1 \right].$$

Thus, U_{OLG} can be thought of as the percent change in the average gain from the current operating point to the calibration point. This function can easily be determined by measuring the combined response of all HLRF stations over the valid range of operating points for a particular cycle. The Direct RF FB loop must be disabled for this measurement.

With this definition of U_{OLG}, and by satisfying the foregoing assumptions, the compensated open loop gain at each individual station becomes:

$$G_{OLG} G_{Sys} = G_{OLG\,nom} G_{Sys\,nom} \cdot \frac{G_{Sys\,N}\left(f, V_{bias}\right)}{G_{Sys\,N}\left(f, V_{bias}\right)\Big|_{Cal}} \cdot \left[1 + \alpha_{OLG} \cdot \left[\frac{\overline{G_{Sys}}_{Avg}\left(f, V_{bias}\right)\Big|_{Cal}}{\overline{G_{Sys}}_{Avg}\left(f, V_{bias}\right)} - 1 \right] \right]$$

If for a particular station $\frac{G_{Sys\,N}\left(f, V_{bias}\right)\Big|_{Cal}}{G_{Sys\,N}\left(f, V_{bias}\right)} = \frac{\overline{G_{Sys}}_{Avg}\left(f, V_{bias}\right)\Big|_{Cal}}{\overline{G_{Sys}}_{Avg}\left(f, V_{bias}\right)}$, then α_{OLG} can be set to unity and $G_{OLG} G_{Sys}$ will equal $G_{OLG\,nom} G_{Sys\,nom}$ for all operating points. However, the price that is paid for using only one program to all stations is that perfect compensation for all stations is not possible at all operating points. Perfect compensation will occur only at points for which

$$\frac{G_{Sys\,N}\left(f, V_{bias}\right)\Big|_{Cal}}{G_{Sys\,N}\left(f, V_{bias}\right)} = \left[1 + \alpha_{OLG} \cdot \left[\frac{\overline{G_{Sys}}_{Avg}\left(f, V_{bias}\right)\Big|_{Cal}}{\overline{G_{Sys}}_{Avg}\left(f, V_{bias}\right)} - 1 \right] \right]$$

Thus, the use of α_{OLG} is to choose the points for which this is satisfied; or in other words to try to optimize the compensation across the operating points given the constraints of how a particular station behaves compared to the average U_{OLG} function. Thus, the calibration of U_{OLG} can be an iterative process. First U_{OLG} can be determined from the combined response of all stations with Direct RF FB loops off. U_{OLG} is then sent to all stations. One by one, each station's α_{OLG} knob can be adjusted such that its gain is relatively constant across the operating points. Then the combined response can be re-measured and U_{OLG} can be retuned to achieve a relatively constant combined response.

The engineering units for U_{OLG} have been defined as a percent of the system gain at the nominal $u_{OLG\,Cal}$ value of 7.5V. This is apparently different from the thought process above that thought of it as a percent offset from the nominal gain; however the difference is slight and merely adds 100% to the equation. In this way, when $U_{OLG} = 0$, a user can interpret the compensated system gain as being equal to (or 100%) of the uncompensated system gain; meaning that no compensation is being applied. As U_{OLG} is tuned negative and positive, the compensated system gain is varied below and above 100% of the uncompensated system gain. The practical minimum and maximum values of U_{OLG} (assuming $\alpha_{OLG} = 1$) are -5V and +5V respectively (the MRF DAC Line Driver output range). The conversion formula from primary units of Volts (V) to engineering units of percent (%) is:

$$U_{OLG}\,(\%) = \left(1 \; + \; \frac{U_{OLG}\,(Volts)}{7.5\,V}\right) \cdot 100\%$$

The above transform has been applied to all ACNET devices associated with RFOLG. The actual response of RFOLG, represented as the percent offset from a nominal response at a control voltage of 7.5 volts, is shown in Fig. 5 below. Also shown in Fig. 5 is the same response on a logarithmic scale. To increase the compensation range, the nominal value of α_{OLG} can be made greater than unity. However, the control voltage must not cause the RVA-2500 (which is the device used to implement the RFOLG function) to enter into a region where its phase response drastically deviates from the nominal phase. Figure 6 shows the relative phase response as a function of U_{OLG}.

The nominal design values of $G_{OLG\,nom}$ and $G_{Sys\,nom}$ are documented in the Variable Gain Amplifier discussion of the MRF Amplitude Regulation Loop section.

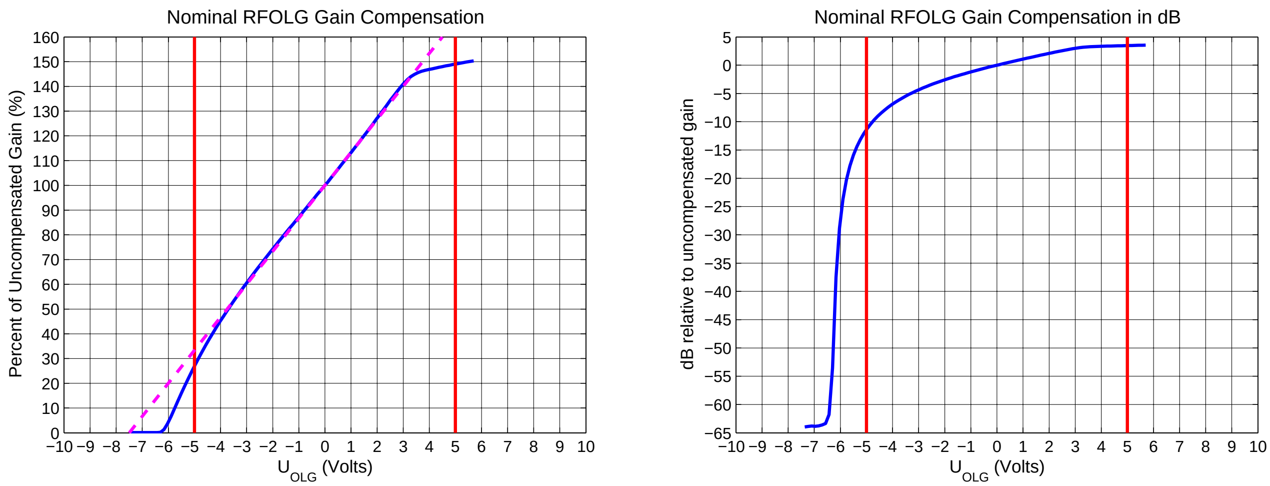


Figure 5: Nominal RFOLG gain compensation in percent (left) and dB (right). Practical domain limits are in red. Also shown on the left is the ACNET database transform in dashed magenta.

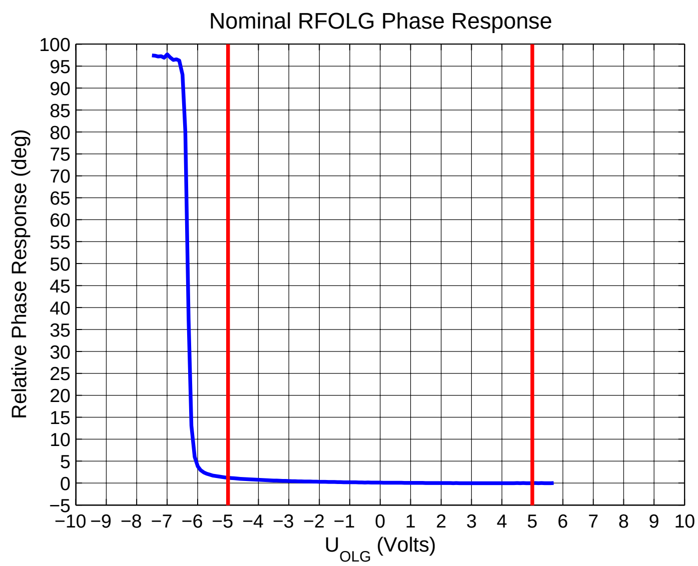


Figure 6: Nominal RFOLG relative phase response. Practical domain limits are in red.

Proof that the RFOLG function works is shown in Figs. 7 and 8 below. These plots were taken at the MI-60 Test Station for a fixed 90 kV voltage request across the 300 kHz frequency sweep typical of a Tclk 23, MI State 05 cycle with both the Direct RF FB loop and the MRF amplitude regulation loop disabled. Figure 7 shows the detected magnitude, I:VSMAGA, and the associated magnitude error, I:VSMERA. The error begins to increase around 0.3 sec. as the frequency begins to ramp from its initial value of ~52.8114 MHz to its final value of ~53.104 MHz. Figure 8 shows how the error has been reduced across the cycle via RFOLG programming.

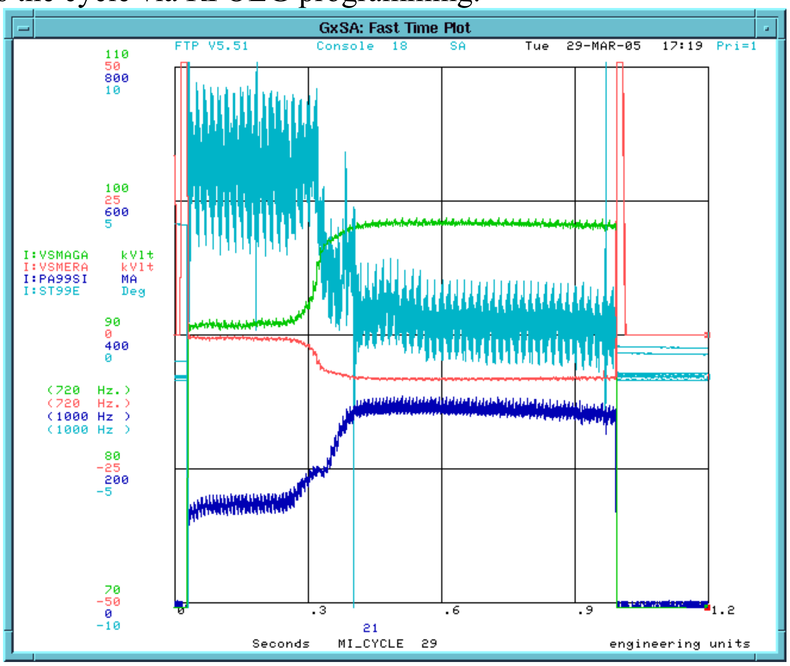


Figure 7: MI-60 Test Station open loop response WITHOUT RFOLG programming.

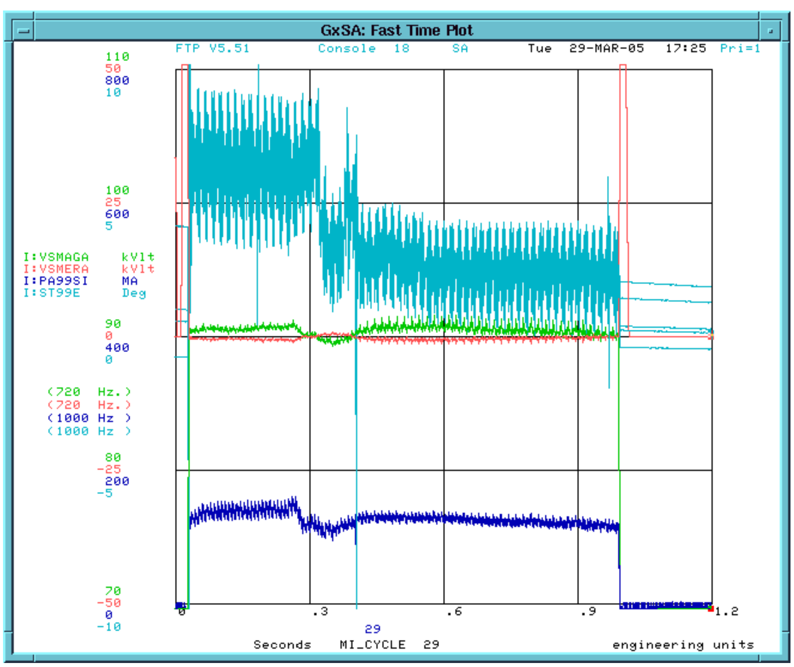


Figure 8: MI-60 Test Station open loop response WITH RFOLG programming.

Grid Bias Offset Program (RFGBP)

The Grid Bias Offset Program deserves a brief discussion to document its role in the RF power amplifier (PA) operation and its impact on the system gain. The PA grid bias voltage is derived via:

$$V_G = \kappa_G \cdot (u_{GB\,Cal} + \alpha_{GBP} U_{GBP}) - 500$$

where

V_G : the PA grid bias voltage in [V].

κ_G : the internal grid bias supply scaling from control volts to PA grid volts. $\kappa_G = 50$.

U_{GBP} : the global Grid Bias Offset Program in [V]

$u_{GB\,Cal}$: the local station adjustable static grid bias voltage control for when $U_{GBP} = 0$. $u_{GB\,Cal}$ is in [V] and is adjusted via a potentiometer at the Anode Modulator's anode and grid bias program adjust module.

α_{GBP} : the local station adjustable scaling of U_{GBP} which allows individual station tuning. α_{GBP} is available as a potentiometer at the Anode Modulator's anode and grid bias program adjust module.

-500: an internal offset applied in the grid bias supply control card. The supply itself is limited from –400 V to 0 V.

The Grid Bias Offset Program provides a means to dynamically adjust the bias point of the PA tube; thus providing control of the transconductance of the tube, the its class of operation, and the its efficiency. Increasing the grid bias closer to 0 V increases the transconductance and brings the PA into Class A operation which is less efficient but linear. Having Class A linear operation simplifies feed-forward beam loading compensation and provides gain to the Direct RF FB loop when the cavity is operating at close to zero gap voltage.

Increasing the transconductance of the tube has a trade off between PA gain and PA efficiency. As the transconductance is increased the PA gain increases thus decreasing the necessary cathode drive power to the tube; however, the PA efficiency is decreased. Thus it is a trade off between available SSD power and both available and dissipated PA tube power.

Ideally, the adjustments provided in the grid bias control should allow all stations to be calibrated for similar behavior. However, it is important to note that once a tube begins to age and its amplification factor begins to decrease, one cannot match both the RF gain and the anode DC bias current. Thus in practice, the grid bias voltage calibration is a compromise between matching the RF gain and maintaining a reasonable DC bias current and anode efficiency. As a first order analysis, one can begin as follows: The cathode current of a tube can be described by the 3/2 power law according to the following expression:

$$I_K = \beta\left(V_G + \frac{V_S}{\mu_S} + \frac{V_A}{\mu_A}\right)^{3/2} = \beta \cdot V_{Bias}^{3/2} \quad .$$

Assuming small variations in V_G and expanding the above into a Taylor series about the biasing point one obtains

$$I_A \cong \beta \cdot V_{Bias}^{3/2} + \frac{3}{2}\beta \cdot V_{Bias}^{1/2} \cdot v_{RF} \sin(\omega t) = I_{DC} + I_{ac} \quad ,$$

if higher order terms are neglected. Thus if the tube amplification factor, β, decreases with tube aging, a compensating change in V_{Bias} cannot match both the DC and ac terms which were associated with the original value of β. For example to match the DC term, the bias voltage would have to be scaled as:

$$V_{Bias\ Aging} = \left(\frac{\beta_{Original}}{\beta_{Aging}}\right)^{2/3} \cdot V_{Bias\ Original} \quad .$$

On the other hand, to match the ac term, the bias voltage would have to be scaled as:

$$V_{Bias\ Aging} = \left(\frac{\beta_{Original}}{\beta_{Aging}}\right)^{2} \cdot V_{Bias\ Original} \quad .$$

Both equations cannot be satisfied simultaneously for $\beta_{Original}$ unequal to β_{Aging} . Thus a compromise must be made. Fortunately, the Open Loop Gain Compensation function (RFOLG) provides a means to compensate for the change in system gain resulting from the change in grid bias.

It is important to remember that RFGBP will change the PA gain, class of operation, and efficiency. The PA gain change affects both the Feed-Forward beam loading compensation loop and the Direct RF FB loop. To minimize the effect on the Direct RF FB loop, the Open Loop Gain Compsation function (RFOLG) should be tuned after tunings of the grid bias offset via RFGBP. For thoroughness, tunings should be made both locally and globally.

Screen Current Regulation Loop

Historically, the screen current regulation loop was used as a crude cavity voltage amplitude controller that worked in conjunction with programming the PA anode voltage. The idea was to force the PA tube to conduct a fixed amount of screen current. This would ensure that the PA anode voltage was dipping into the PA screen voltage. Taking into account the anode to gap voltage step-up, the cavity gap voltage is then directly related to the anode DC bias, under the condition of drawing screen current, by the formula:

Screen Current Condition

$$v_{Gap} \cong (V_A - V_S) \cdot N_{gap}$$

V_A: the PA anode DC bias voltage

V_S: the PA screen DC bias voltage

N_{gap}: the cavity gap to anode voltage ratio

Thus, historically, the cavity gap voltage was controlled by programming the PA anode DC bias via the anode modulators while simultaneously forcing screen conduction via the screen current regulation loop. Besides acting as a cavity voltage controller, it also helped to keep the PA tube running efficiently.

The motivating factors to move away from screen current regulation include:

- There is now a Direct RF FB loop that can perform cavity voltage control. In the historic architecture, the screen current regulation scheme is the ultimate cavity voltage amplitude control at an individual station. The Direct RF FB can now perform this task. The screen current regulation loop can still be used as a limiter to reduce the RF drive if large screen current develops.
- Operating the PA tube away from saturation (screen current condition) increases the headroom and linearity for the RF feed forward beam loading compensation
- With the historic regulation, low cavity voltage implies low anode voltage. This implies that the anode modulator series tube provides its largest voltage drop at low cavity volts. Coupled with increased anode current demands for beam loading compensation, the anode modulator series tube power dissipation at low cavity volts is a limiting factor for low voltage operation if historic screen current regulation is used. Moving away from screen current regulation would allow power sharing between the anode modulator series tube and the PA amplifier tube.
- Reducing peak turn on transients and overshoot

During the course of the MRF development, the Screen Current Regulation modules were modified to provide the capability to move away from the historic screen current regulation scheme. The modifications reduced the control limits of the screen current regulation loop. The positive control was limited to +3% of the program request. The negative control limit was limited to –60% of the program request. Previously these limits were +70% and –70%. Reducing the positive limit to +3% greatly reduced turn on transients and overshoot problems. It also minimized the offset that the screen current regulation module adds to the raw cavity voltage request coming from the MRF. A simple offset destroys linearity of a system; thus minimizing the offset helps to keep the resultant cavity voltage directly proportional to the request. Leaving a larger negative limit still allows for the screen current regulation to reduce the RF drive if it is too large.

Referring to the block diagram in Fig. 1, it is important to remember that the screen current regulation module provides a means to adjust, via a front panel accessible potentiometer, the level of screen current which is considered the zero error point for the screen current regulation loop. This setpoint is the level below which the screen current regulation module will want to increase the RF drive and above which it will want to reduce the RF drive.

Up to this point, the details of the RF drive level control have not been discussed. The RF drive level, v_{Drive}, is controlled via a variable gain amplifier (VGA) represented by G_{VGA} in the block diagram. Since the VGA design is closely linked to the global amplitude control, its details will be considered in the discussion of the MRF amplitude regulation loop.

MRF Amplitude Regulation Loop

The MRF amplitude regulation loop is responsible for regulating the sum voltage of a group of cavities. For Stage I, the historic architecture of two groups of 9 cavities, Group A and Group B, is preserved. Referring to the MRF system block diagram of Fig. 1, the MRF amplitude controller processes a user voltage request and provides the global HLRF station cavity voltage request to each station within each group of cavities. Presently, to preserve the historic architecture of the anode modulator programming, the MRF station cavity voltage request not only generates the solid-state drive (SSD) program, U_{SSD}, but also the anode program, U_{APG}. A more detailed diagram of the actual MRF SWH code which implements the amplitude regulation loop is shown in Fig. 9 on the following page.

➢ *The Anode Program (APG)*

Unlike the historic CAMAC interpretation of I3 parameter page h588 RFSUM voltage requests, the MRF system correctly calculates the appropriate PA anode DC bias needed to make an individual cavity gap voltage. As discussed in the 'Screen Current Regulation Loop' section, the cavity gap voltage is related to the PA anode DC bias via the equation $v_{Gap} \cong (V_A - V_S) \cdot N_{gap}$. This implies that given a station cavity voltage request, $v_{Cav\,req}$ in units of (kV) from the MRF system, the minimum PA anode DC bias should be,

$$V_A = \frac{v_{cav\,req} + V_S\; N_{gap}}{N_{gap}} \quad .$$

V_A is realized via the anode modulator using a scaled version of U_{APG}, the global anode program control signal from MRF. The scaling is via both: (1) the individual station adjustment knob represented by α_{APG}, nominally equal to 0.75, and (2) the anode modulator transfer function, represented as κ_A (nominally 3 [kV/V]), which converts the anode program into the actual anode modulator output volts to the PA anode. Taking this into account, the MRF U_{APG} output in [V] is related to $v_{Cav\,req}$ in [kV] via:

MRF SWH Anode Program Output Transfer Function:

$$U_{APG} = \frac{v_{cav\,req} + \Delta_{APG}}{\chi_A} \quad \text{[V]}$$

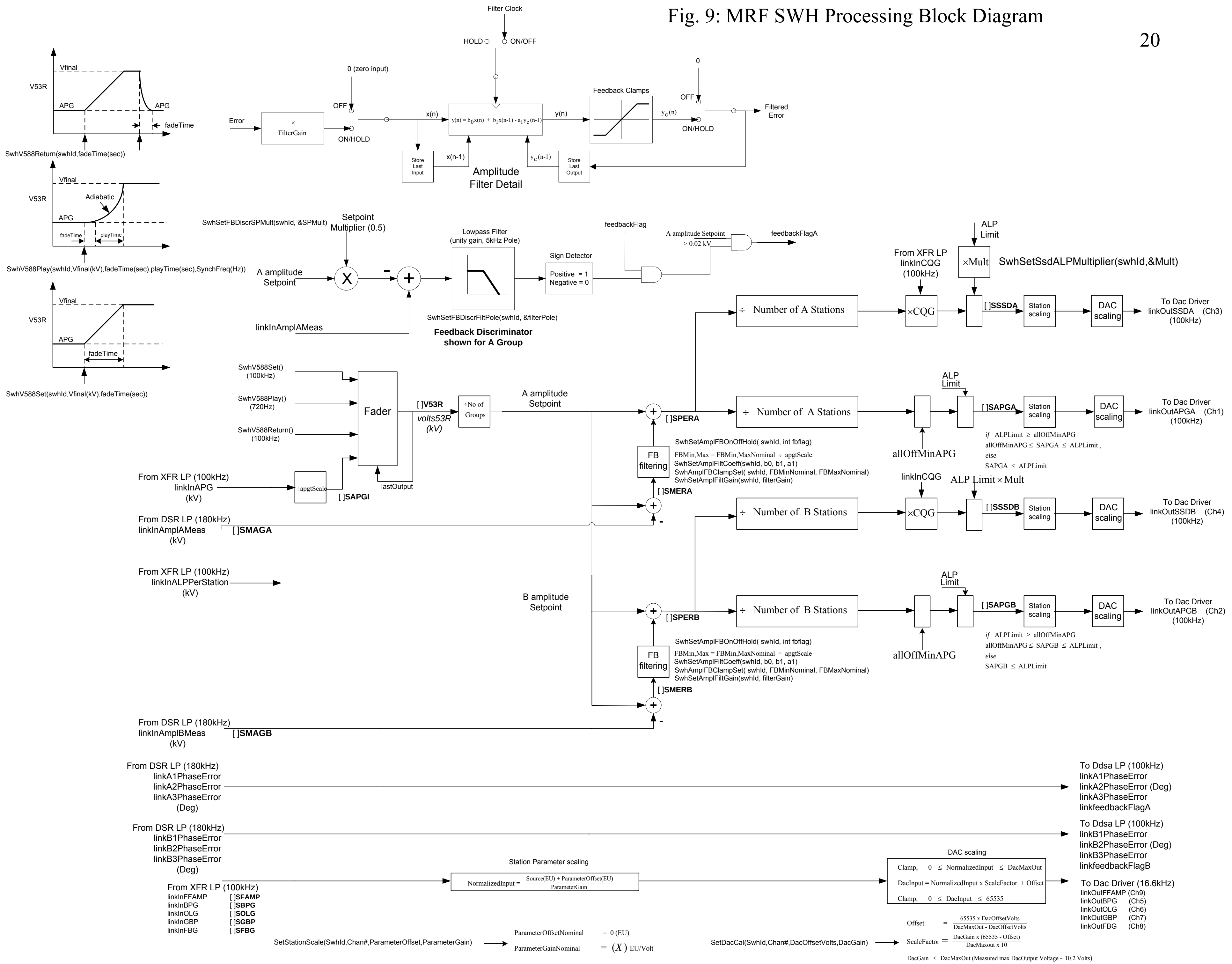
where:

$\chi_A = \kappa_A \alpha_{APG} N_{Gap} = 27.5625$ [kV/V] is the MRF SWH 'parameter gain'

$\Delta_{APG} = V_S \cdot N_{Gap} = 12.25$ [kV] is the MRF SWH 'parameter offset'

The value of N_{Gap} used was 12.25. This value was determined from MI-60 test station measurements and from results of the SSD upgrade installation of 2004.

Fig. 9: MRF SWH Processing Block Diagram



The APG program has both a minimum and a maximum limit. The minimum limit, 'allOffMinAPG', is used to keep the PA tubes 'alive' with anode bias during zero voltage requests. The maximum limit is defined by ALP which is discussed next.

➢ *The Anode Limit Program (ALP)*

The ALP function is meant to protect the HLRF cavities predominantly from tuner sparks which can occur at a voltage threshold that is frequency dependent. The protection is achieved through saturation of the PA tube. The maximum RF anode voltage swing is limited by the anode voltage bias of the PA tube. Through the cavity gap to anode step-up ratio, this also limits the maximum cavity gap voltage that can be achieved.

Applying the ALP limiting to the APG program in MRF preserves the historic anode limiting function. Since the historic ALP has been defined in units of raw anode program volts a conversion formula is needed relating the single station cavity gap voltage limit, $v_{Cav\,Limit}$, to the ALP. The formula is:

$$v_{Cav\,Limit}\,[kV] \;=\; 27.5625 \cdot ALP\,[V] \;-\; 12.25$$

$v_{Cav\,Limit}\,[kV]$	: the single station cavity gap voltage limit in kV
$ALP\,[V]$	: the Anode Limit Program in raw I3 or C465 units of V

The MRF XFR module performs this scaling on the raw ALP units before shipping ALP to SWH in units of kV. The above formula is derived from:

$$v_{Cav\,Limit}\,[kV] \;=\; \left[\alpha_{APG} \cdot \kappa_A \cdot ALP\,[V] \;-\; V_S\right] \cdot N_{Gap}$$

with:

α_{APG} :	the station Anode Modulator Program Adjust scaling factor = 0.75 nom.
κ_A :	the station Anode Modulator transfer function scaling = 3 kV/V nom.
V_S :	the PA screen voltage, 1 kV
N_{Gap} :	the average cavity gap to anode voltage ratio = 12.25

The above formulas determine a single station cavity voltage limit. In order to determine the total h588 voltage limit (RFSUM) multiply the above by 18. The I3 primary application page does just that to perform error checking that warns if a user tries to tune the h588 voltage request (via APG) above the RFSUM limit as determined from 18 times the single station voltage limit implied by ALP.

If it is desired to run the anode bias higher than the level which affords cavity protection via PA tube saturation, then another means of cavity protection will need to be employed. This ALP limit can still be applied to the SSD Program in order to limit the RF drive. It is advised that the naming convention be rethought at that time; i.e. ALP can be relabeled to reflect that it is a SSD program limit or the single station cavity voltage limit. The initial MRF design has included SSD program limiting based upon a scaled version of ALP. The scaling is command line adjustable.

➢ *The Solid State Drive Program (SSD)*

With the MRF amplitude regulation loop open, the single station cavity gap voltage request, $v_{Cav\,req}$, is generated from the global h588 (53MHz) system voltage request, v_{53R}, via the following equation:

$$v_{Cav\,req} = \frac{v_{53R}}{num_{Grp} \cdot num_{Sta}}$$

v_{53R} :	the global h588 system voltage request in (kV)
num_{Grp} :	the number of cavity groups used to make the h588 voltage request; equal to 2 for Stage I (2x9)
num_{Sta} :	the number of stations per group; 9 for Stage I (2x9)

Currently for Stage I (2x9) slip-stacking, the num_{Sta} value changes from 9 to 2 during the slipping process which leaves 2 stations per group on and turns 7 stations per group off.

Currently, the global h588 voltage request, v_{53R}, can be set via the 'Fader' through I6 parameter page sequence table messages. The messages and the 'Fader' determine how v_{53R} is generated. Using the I6 message 'V588APG(t)' returns v_{53R} to be equal to the historical I3 APG(t) Curve (I:RFAPG). An additional functionality provided by MRF is to instantaneously (within a 100kHz tic) set v_{53R} to a constant request via the 'V588Set' I6 message. This is useful for slip-stacking at the beginning of slipping and at recapture. Furthermore, the 'V588Play' I6 message provides an adiabatic change from the present value of v_{53R} to a final value of v_{53R}.

The single station voltage request, $v_{Cav\,req}$, is sent to each HLRF station via the global solid-state drive program (SSD), U_{SSD}. At each HLRF station, U_{SSD}, is scaled via a SSD Program Adjust Module and processed by the screen current regulation loop to generate the individual station SSD program control signal, u_{SSD}, which in turn is used by the variable gain amplifier (VGA) to generate the RF drive level, v_{Drive}, to the Direct RF FB loop; ultimately creating the station cavity gap voltage, v_{Gap}.

For the remaining discussions, it is assumed that the screen current regulation loop is tuned for zero error such that it does not affect the station SSD program, u_{SSD}. Under this condition the effect that the screen current regulation has on the MRF amplitude loop is minimized as was discussed in the screen current regulation loop section. In practice, zero screen current error is not achieved under all conditions; however, it should be strived for at the station calibration point.

➢ *The Historic RFCQG Function*

The historic RFCQG (RF Cascode Q Gain) function has been preserved in the MRF architecture as a multiplier on the SSD program as seen in the main block diagram of Fig. 1. Although the original intent of the RFCQG function was to compensate for known changes in the HLRF system gain, similar to the new RFOLG function, its original function as a true feed-forward compensation term was not preserved in the strictest sense with the introduction of the Direct RF FB loop which was placed physically after the RFCQG function location. A true feed-forward compensation term should be placed inside a feedback loop. In order to minimize the impact on operations during the MRF development, the historic RFCQG function was preserved and the new RFOLG function was initially introduced as a static value.

The original scaling for RFCQG as a multiplication factor to SSD was investigated during the MRF development in order to understand the necessary scaling needed within MRF. As shown in Fig. 1, RFCQG in MRF is incorporated as:

$$v_{Cav\,req_{RFCQG}} = 0.5 \cdot RFCQG \cdot v_{Cav\,req}$$

where $v_{Cav\,req_{RFCQG}}$ is the RFCQG scaled version of $v_{Cav\,req}$. Thus, MRF can be run in open loop and still provide the RFCQG function. To effectively remove the RFCQG multiplication in closed loop the RFCQG curve should be made equal to 2 for the duration of the entire cycle. Caution must be used to ensure that RFCQG is properly used so that it is not applying an unwanted dynamic scaling of the MRF amplitude loop gain in closed loop since it sits inside the MRF amplitude loop.

➢ *The Variable Gain Amplifier (VGA)*

From the preceeding discussions, the VGA provides the necessary RF drive level, v_{Drive}, to the Direct RF FB loop in order to generate a single station cavity gap voltage, v_{Gap}, which ideally should equal the MRF request, $v_{Cav\,req}$. From the MRF block diagram in Fig. 1, the VGA modifies the available station RF input level, v_{in}, to make v_{Drive}. Its gain, G_{VGA}, is controlled by, and thus is a function of, the station SSD program, u_{SSD}. Ideally, for the cavity gap voltage to be directly proportional to the request, the VGA gain should be a strict linear transform of u_{SSD}.

Definition of the VGA Gain:

$$G_{VGA}\left(u_{SSD}\right) = m_{VGA} \cdot u_{SSD} = \frac{v_{Drive}}{v_{in}}$$

u_{SSD} : the local station SSD program which controls the VGA gain.
v_{in} : the RF input level applied to the Station RF Controller
v_{Drive} : the RF drive level inside the Station RF Controller immediately before its 'drive + error' summing junction (at J3 of its schematic)
G_{VGA} : the gain of the VGA from v_{in} to v_{Drive}
m_{VGA} : the ideal slope of the VGA gain as a function u_{SSD}.

The design value of m_{VGA} is determined from v_{in} and the designed relationship between the cavity gap voltage request made via u_{SSD} and the actual cavity gap voltage achieved via v_{Drive}.

Referring again to the system block diagram of Fig. 1 and assuming that the Direct RF FB loop is performing its job of forcing $v_{Gap} = G_{OLG\,nom} G_{Sys\,nom} v_{Drive}$, as previously discussed in the *Direct RF FB Loop Steady-State Design Equations* section, the overall relationship from $v_{Cav\,req}$ to v_{Gap} is defined as:

MRF Request to Cavity Gap Relationship:

$$v_{Gap} = v_{Cav\,req} \cdot \frac{\alpha_{SSD}}{\chi_{SSD}}\, m_{VGA}\, v_{in} \cdot G_{OLG\,nom} G_{Sys\,nom}$$

where

$\alpha_{SSD} = \dfrac{u_{SSD}}{U_{SSD}} \leq 1$: is an individual station adjustment scaling applied via the SSD Program Adjust Module to the global SSD Program, U_{SSD}, in order to generate the station SSD Program, u_{SSD}. (Note, as previously mentioned, it is assumed here that the Screen Current Regulation Loop does not effect the SSD Program.)

$\chi_{SSD} = \dfrac{v_{Cav\,req}}{U_{SSD}}$: is the MRF SWH output scaling 'parameter gain' used to make the MRF digital-to-analog (DAC) output volts for U_{SSD} from the MRF single station cavity voltage request, $v_{Cav\,req}$.

For $v_{Gap} = v_{Cav\,req}$, the ideal design value for m_{VGA} is given as:

$$m_{VGA} = \frac{\chi_{SSD}}{v_{in} \cdot \alpha_{SSD} \cdot G_{OLG\,nom} G_{Sys\,nom}}$$

The MRF SWH Output Scaling, χ_{SSD} :

The design value for χ_{SSD} is based upon providing enough headroom in the MRF DAC output and keeping the MRF DAC output below its maximum 10V output and within a reasonable range that can correspond to the expected cavity voltage requests.

The present maximum single cavity voltage imposed by the Anode Limit Program (ALP) is 240 KV (ALP=9.9v, see *The Anode Limit Program* section for the scaling factor). The present operational maximum single cavity voltage request of ~206 kV can be found during the normal stacking cycles. The present operational minimum single cavity voltage request of ~30kV can be found during coalescing on the Tclk 2A and 2B cycles. The absolute minimum single cavity voltage is imposed by the anode modulator which does not release a SSD inhibit to the SSD amplifiers until the modulator output voltage exceeds a threshold of ~3kV; which corresponds to 21.5 kV to 24 kV depending upon the cavity gap-to-anode ratio. For the system design and the VGA specifications, 20 kV is taken as the minimum single cavity voltage request.

The minimum positive headroom that is available to the MRF DAC output will occur at the maximum single cavity voltage request, denoted as $v_{Cav\,req\,\max}$ and is calculated as:

$$\text{Minimum MRF Positive Headroom: } h_{MRF} = \frac{V_{DAC\,\max} - U_{SSD}(v_{Cav\,req\,\max})}{U_{SSD}(v_{Cav\,req\,\max})} \cdot 100\%$$

where $V_{DAC\,\max}$ is the maximum MRF DAC output voltage, or 10V. Typically, $v_{Cav\,req} = \dfrac{v_{53R}}{num_{Grp} \cdot num_{Sta}}$ where $num_{Sta} = 9$ (see *The Solid State Drive Program* section); however, when there are fewer stations available per group due to a station tripping or being off, $v_{Cav\,req}$ is increased. Thus, the positive headroom required to support having only num_{Sta} stations available is:

$$\text{Required MRF Positive Headroom for } num_{Sta}: \quad \left(\frac{9}{num_{sta}} - 1\right) \cdot 100\%$$

For $num_{Sta} = 8$ this is 12.5%.

Note: The Anode Limit Program (ALP) is the ultimate limit on the available positive headroom since it limits the cavity voltage that can be requested by MRF. Also note that the minimum positive headroom is defined for $v_{Cav\,req\,\max}$; for practical operating levels which are lower than $v_{Cav\,req\,\max}$ the headroom is greater.

The SSD Program Adjust Scaling, α_{SSD} :

The positive headroom available in the local station SSD program is controlled via α_{SSD} through the SSD Program Adjust module. When α_{SSD} is maximized to 1, the maximum headroom is determined from its nominal setting, $\alpha_{SSD\,nom}$, as:

$$\text{SSD Program Adjust Positive Headroom: } h_{SSD} = \left(\frac{1}{\alpha_{SSD}} - 1\right) \cdot 100\%$$

For $\alpha_{SSD\,nom} = 0.75$, this is 33.3%

It is important to note that α_{SSD} is not a linear function of the SSD Program Adjust knob. This is due to the fact that the Screen Current Regulation module, which is the module immediately following the SSD Program Adjust module, does not have a high input impedance. The relationship between α_{SSD} and the SSD Program Adjust knob is shown in Fig. 10 below.

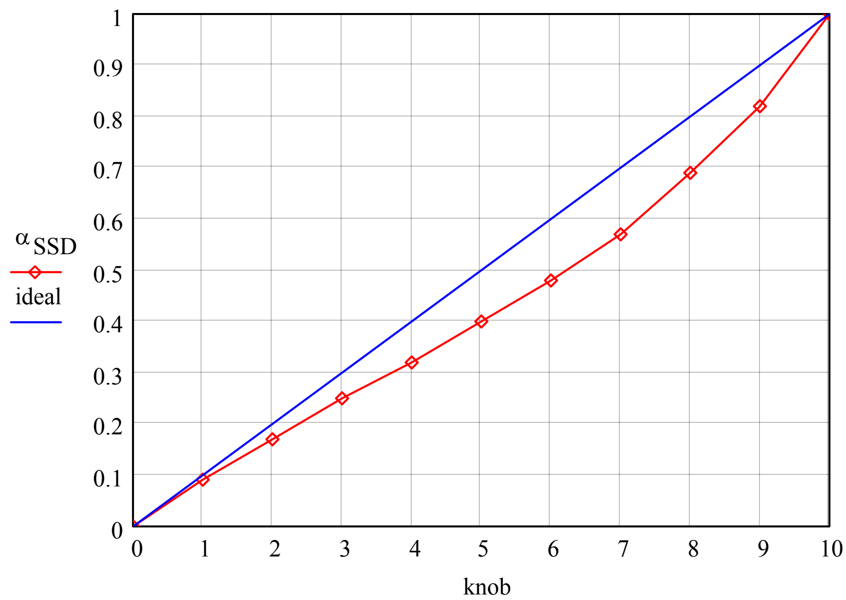


Figure 10: SSD Program Adjust Module Scaling vs. Knob Setting

VGA Specifications Summary:
In addition to the VGA specifications arising from the above discussions, the VGA should also be non-dispersive and have a group delay that remains constant as a function of u_{SSD}; in other words, its phase, ϕ_{VGA}, should satisfy,

$$\phi_{VGA} = \omega \cdot t_{delay} \quad \text{where } t_{delay} \text{ is a constant.}$$

The following page summarizes the VGA specifications and quantifies the scaling factors and available headroom that were introduced in the previous discussions. 220 kV was taken as the single cavity voltage request that corresponds to 9V from the MRF DAC. This provides enough headroom from the practical operating level of ~206 kV while also staying close to the ultimate ALP cavity voltage limit at 10V from the MRF DAC. The scaling factors documented here are the design values. There should be enough headroom in the various components in case the scaling factors need to be changed as experience with the system is gained. If they should need to be changed, the discussion documented here should prove to be useful. A new VGA was designed during the MRF project to meet these specifications.

It is extremely important to remember that G_{VGA} is the product of the gain through the VGA module itself, any attenuators between the VGA module and the Station RF Controller's RF Board, and the attenuation from the RF input to the 'drive+error' summing junction on the Station RF Controller's RF Board. Thus, the calibration of the VGA module must take place with the VGA installed and must include the measurement from the VGA module input to the 'drive+error' summing junction on the RF Board.

Specifications for the VGA Design

$$G_{VGA} = m_{VGA} \cdot u_{SSD} \quad \text{for} \quad u_{SSD\,\min} \le u_{SSD} \le u_{SSD\,\max}$$

where:

$$m_{VGA} = \frac{\chi_{SSD}}{v_{in} \cdot \alpha_{SSD} \cdot G_{OLG\,nom} G_{Sys\,nom}}$$

$$\chi_{SSD} = \frac{v_{Cav\,req}}{U_{SSD}}$$

$$\alpha_{SSD} = \frac{u_{SSD}}{U_{SSD}}$$

$$\phi_{VGA} = \omega t_{delay} \quad \text{where} \quad t_{delay} = \text{constant}$$

Minimum MRF Positive Headroom: $h_{MRF} = \dfrac{V_{DAC\,\max} - U_{SSD}(v_{Cav\,req\,\max})}{U_{SSD}(v_{Cav\,req\,\max})} \cdot 100\%$

SSD Program Adjust Positive Headroom: $h_{SSD} = \left(\dfrac{1}{\alpha_{SSD}} - 1\right) \cdot 100\%$

Maximum VGA output (dBm): $v_{Drive\,\max} = 20 \cdot \log(m_{VGA} \cdot u_{SSD\,\max}) + v_{in}[dBm]$

Nominal System Design Parameters		
Parameter	**Value**	**Units**
$v_{cav\ req\ min}$	20	kV
$v_{cav\ req\ max}$	220	kV
$U_{SSD}(v_{cav\ req\ max})$	9	V
$V_{DAC\ max}$	10	V
α_{SSD}	0.7	V/V
G_{OLG}	6.7	dB
G_{sys}	105	dB
v_{in}	7	dBm

Specifications		
Specification	**Value**	**Units**
χ_{SSD}	24.444	kV/V
h_{MRF}	11.11	%
h_{SSD}	42.86	%
v_{in}	0.708	V_{pk}
m_{VGA}*	0.128	1/V
$u_{SSD\ min}$	0.57	V
$u_{SSD\ max}$	10	V
$v_{Drive\ max}$*	9.2	dBm

* It is important to note that the gain term, G_{VGA} , includes approx. – 4dB from the Station RF Controller RF Board components (RF input up to drive+error summing junction); thus, the specifications for the VGA itself have to be increased by 4dB. The nominal G_{OLG} assumes the 'Drive+Error' limiter is set to 8.0v and u_{OLG}=7.5v .

Note: the percent headroom is defined using $v_{Cav\ req\ \max}$.

The achieved typical VGA magnitude and phase response is shown in Figs. 11 and 12 below. This is actual data from the VGA upgrade installation into the Station RF Controllers.

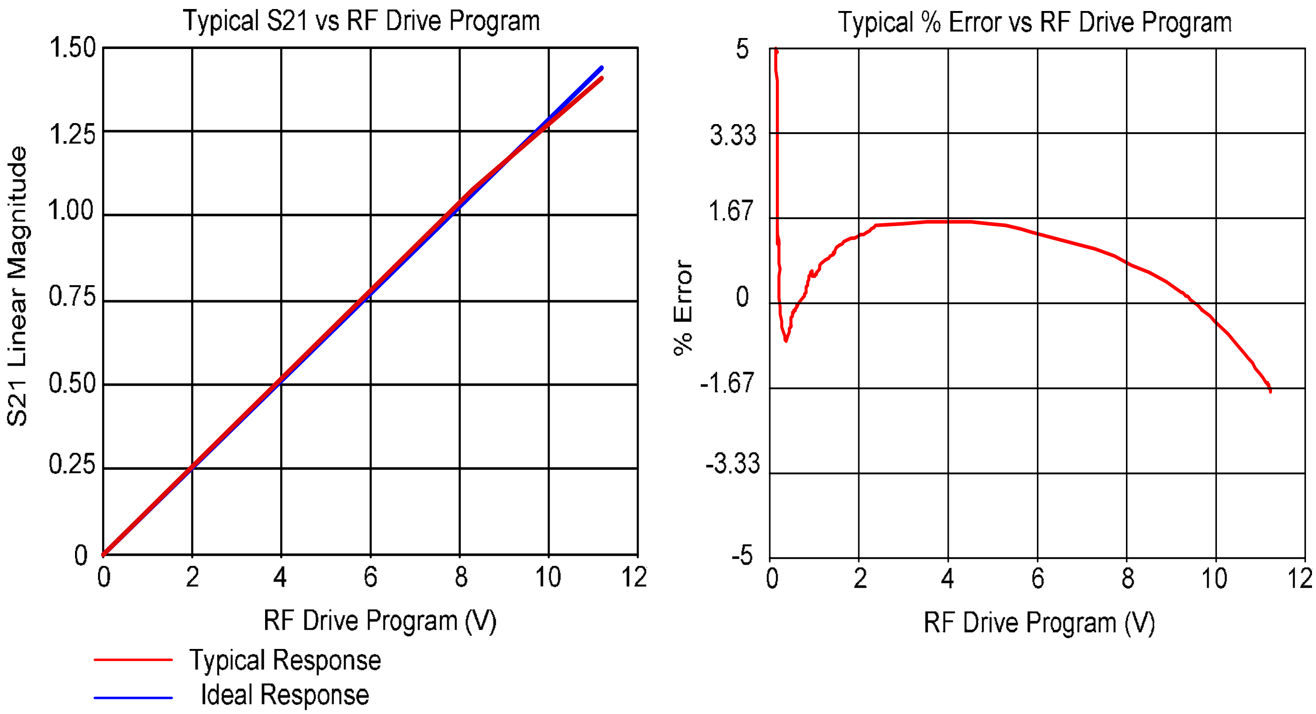


Figure 11: The typical VGA magnitude response from the RF Input to J3 of the Station RF Controller for a +7dBm RF Input level (left). The ideal response shown is the specified slope of 0.128. The typical percent error is shown on the right.

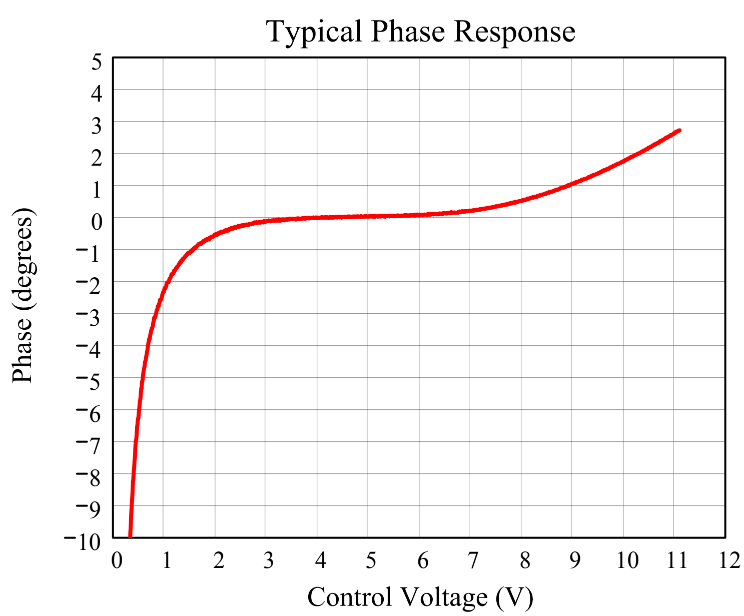


Figure 12: The typical VGA relative phase response.

➢ *MRF Amplitude Feedback Zero Error Condition & A/B Pots*

Similar to the Direct RF feedback loop, the control effort of the MRF amplitude feedback loop is minimized if the system is calibrated to nominally have a zero MRF amplitude error, denoted as $v_{Grp\,Error}$ in the main block diagram of Fig. 1, in open loop. This simply means that the measured group voltage, $v_{Grp\,Meas}$, should equal the requested group voltage, $v_{Grp\,req}$. The requested group voltage is simply the global h588 system voltage request, v_{53R}, divided by the number of groups, num_{Grp}.

The measured group voltage, $v_{Grp\,Meas}$, is derived from a vector sum of all the cavities within that particular group. Ideally, it should equal the actual group voltage, denoted as $v_{Grp\,actual}$ for this discussion, and be determined by a beam based calibration method; however, until this method is developed the scaling factors of the components and cabling that contribute to its value will be used. These scaling factors have been summarized as follows:

- β_{Sta} : the average single station scaling from the cavity gap voltage to the fanback module chassis in the MI-60 control room. It includes the downstream cavity gap monitor, the cabling between the cavity in the tunnel and the gallery Equipment Rack, any splitters, and the cabling between the Equipment Rack and the fanback module chassis.
- β_{Grp}: the average single station scaling through the fanback module chassis to the attenuator in front of the MRF digital signal receiver (DSR). It includes the attenuation through the fanback module chassis and the cabling between the fanback chassis and the attenuator in front of the DSR.
- $\beta_{DSR\,atten}$: the scaling factor representing the attenuator in front of the DSR. The attenuator's main purpose is to ensure that the feedback signal is below the maximum DSR input level of 1.1 Vpk. It can be used as a crude adjustment of the overall scaling as long as its main purpose is still served.
- $\beta_{DSR\,IQ}$: the internal DSR scaling factor between the DSR input signal and the detected magnitude output. The A/D converter output is a 14-bit signed number. The I/Q magnitudes are both 16-bit signed numbers and have a gain term from a detection filter. The magnitude is calculated from the sum of the squares of I and Q.
- $\beta_{DSR\,Pot}$: a fine-tune adjustable (via ACNET) internal scaling factor used for calibration. It is meant to replace the historic manual "A/B Pots". The ACNET devices for Stage I (2x9) are I:VAPOT and I:VBPOT for Group A and B respectively.

Assuming that the product, $\beta_{Sta} \cdot \beta_{Grp}$, is the same for each station (a reasonable assumption that can be made from a thorough system calibration) the measured group voltage can be expressed as:

$$v_{Grp\,Meas} = v_{Grp\,actual} \cdot \beta_{Sta}\beta_{Grp}\beta_{DSR\,atten}\beta_{DSR\,IQ}\beta_{DSR\,Pot}$$

Obviously, for $v_{Grp\,Meas}$ to equal $v_{Grp\,actual}$, the combination of all scaling factors should equal unity:

$$\beta_{Sta}\beta_{Grp}\beta_{DSR\,atten}\beta_{DSR\,IQ}\beta_{DSR\,Pot} = 1$$

In practice β_{Sta}, β_{Grp}, and $\beta_{DSR\,IQ}$ are fixed. $\beta_{DSR\,atten}$ is the first to be adjusted to ensure that the maximum DSR input level is not exceeded at the maximum cavity group voltage. $\beta_{DSR\,Pot}$ is the last to be adjusted. It is the final calibration knob. It is intended to replace the historic manual "A/B Pots" adjustment that is often used for tuning for proton and pBar coalescing.

The zero error condition, $v_{Grp\,Meas} = v_{Grp\,req}$, thus ensures that the actual cavity group voltage is equal to the request. If this is satisfied in open loop, as best as is practically achieved, then the closed loop control effort is minimized. Ideally, each station should be calibrated to contribute equally to the cavity group voltage. This is achieved in practice through the tuning of the Direct RF FB loop and the SSD Program Adjust scaling, α_{SSD}. For a given global SSD program, U_{SSD}, corresponding to a single station cavity gap voltage request, α_{SSD} and the Direct RF FB loop are tuned to ensure that the actual cavity gap voltage achieved is equal to the request. If all stations are calibrated in this way, then the MRF amplitude feedback loop zero error condition will be satisfied in open loop. The Direct RF FB loop is calibrated first to follow the correct procedure of tuning the innermost loops first and the outermost loops last.

➢ *The MRF Amplitude Feedback Filter*

The closed-loop behavior of the MRF amplitude regulation loop can be controlled via the MRF amplitude feedback filter. A detail of the filter has been extracted from the MRF SWH block diagram and is shown in Fig. 13 below.

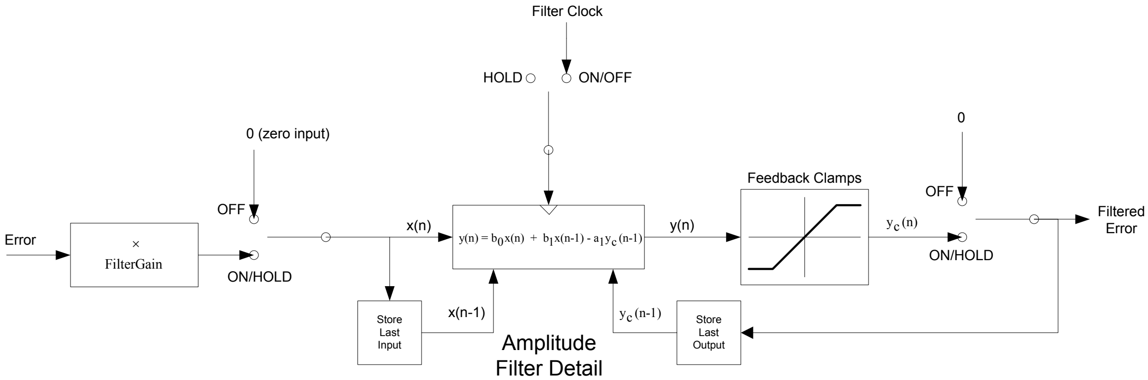


Figure 13: The MRF amplitude feedback filter

The main filter block in the center is a single pole unity gain IIR filter whose coefficients can be changed at the MRF command-line. A 20Hz pole was typically used for the MRF studies during development. The sample rate (filter clock rate) is 100 kHz. The filter gain can be adjusted via the I6 sequence table 'V588Feedback' message. The gain can be monitored via ACNET device I:VAFBG.

The filter output is clamped to a maximum and minimum value that is based on the number of stations used in each group. This is an attempt to minimize 'integrator windup' and to place limits on the control effort that the MRF amplitude feedback loop can apply to the system. The default clamp values are defined in code and have initially been set to +540kV and –450kV for the maximum and minimum values respectively. These values assume 9 stations per group and thus correspond to +60kV per station and –45kV per station respectively. These clamps are roughly +25% and –20% of the nominal 244kV single station maximum cavity voltage request via U_{SSD} and U_{APG}. The clamp values change dynamically with the I6 V588 messages to maintain a constant per station limit based upon the number of stations that are active as determined from the V588 mode (all ON, 4ON/14OFF). The defined clamp values can be changed at the MRF command line.

There are three modes of operation for the filter: ON, OFF and HOLD. In both the ON or OFF mode the filter output is computed in each sample period. However, in the OFF mode the input and the output of the filter are set to 0; thereby disabling the filter from providing a control effort to the loop. In the HOLD mode the entire state of the filter is held; thus, the output of the filter is held constant and the filter is not computed.

Additional state handling of the filter is included in the SWH code to change the output of the filter across station modes (i.e. allON to 4ON/14OFF) in a manner that attempts to keep the same amount of control (as a percentage of the request) immediately after switching to a new number of stations.

➢ *The MRF Feedback On/Off Discriminator*

In order to minimize peak turn-on transients, a Feedback On/Off Discriminator was implemented. A detail of the discriminator (as extracted from the SWH block diagram) is shown below in Fig. 14.

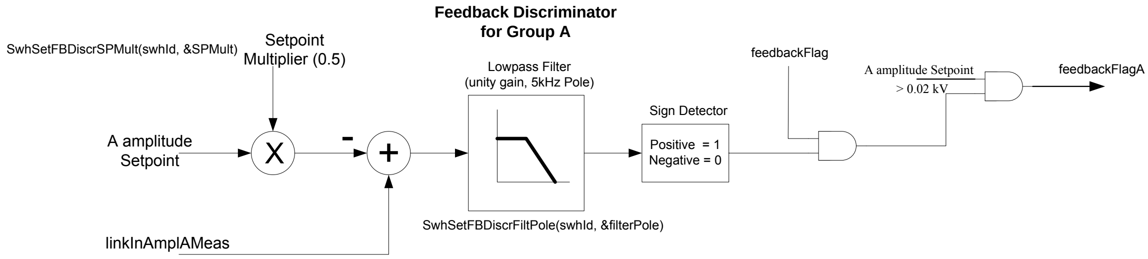


Figure 14: The MRF amplitude feedback filter On/Off Discriminator

Even if the amplitude feedback is requested to be ON (via ‘feedbackFlag’), it is not allowed to turn on unless the following conditions are met: (1) the detected magnitude feedback signal is within a specified fraction of the request, and (2) the request is well above the noise floor of the magnitude detection.

Condition (1) allows the HLRF system to respond to a request before feedback begins to force it equal to the request. This greatly minimizes peak turn-on transients. The specified fraction of the requested voltage is implemented via the ‘Setpoint Multiplier’ which can be adjusted at the MRF command line. The implementation shown in Fig.12 applies a low-pass filter to the difference between the detected magnitude and the ‘Setpoint Multiplier’ version of the request before detecting the sign of this difference. The low-pass filter is meant to eliminate any feedback on/off chattering as the detected magnitude passes from being less than to greater than the ‘Setpoint Multiplier’ version of the request. The pole of the low-pass filter has been initially set to 5 kHz as determined from MRF studies. It can be adjusted at the MRF command line. The default ‘Setpoint Multiplier’ is 0.5 which was also determined via MRF studies. Proof of the discriminator’s effectiveness is shown in Fig. 15 below.

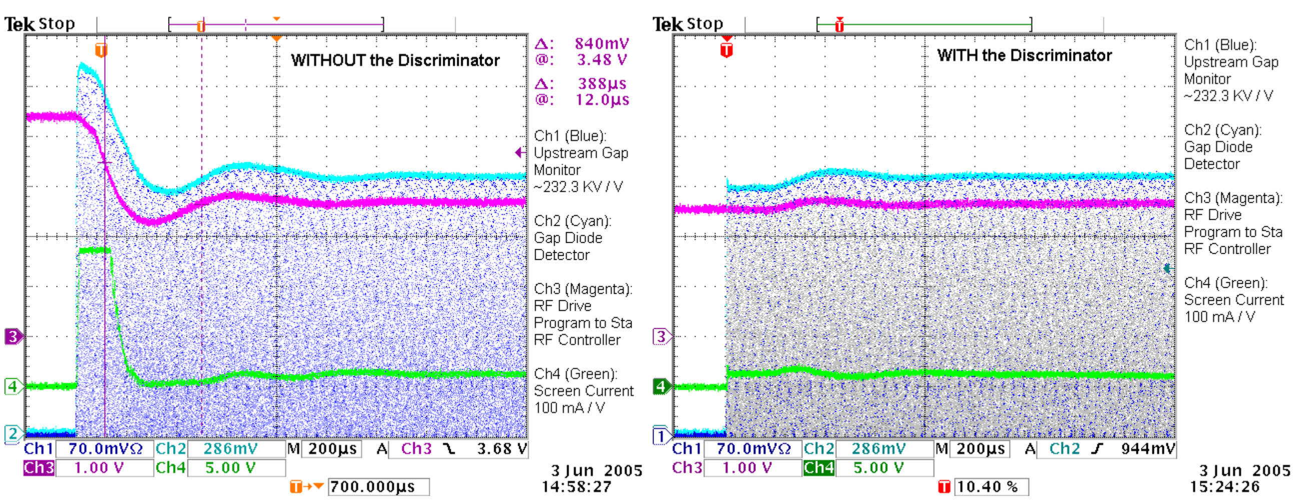


Figure 15: Contrast of WITHOUT and WITH the On/Off Discriminator at the MI-60 Test Station.

Phase Regulation System

The main focus of this section is to document the MRF phase regulation system. However, for completeness, it is worth noting down the various phase control loops which exist in the MI h588 RF system. Again, in order of innermost loop to outermost loop they are:

- Cavity Tuning Control Loop
- Direct RF FB Loop
- Local Station Phase Control Loop
- MRF Phase Control Loop
- LLRF (low-level RF) Beam Phase-Locked-Loop and Radial Position Loop

Again, similar to the amplitude regulation system, these phase loops should be calibrated from innermost loop first to outermost loop last. Three of them are already shown in the main block diagram of Fig. 1: the Direct RF FB Loop, the Local Station Phase Control Loop, and the MRF Phase Control Loop. The other two are briefly mentioned in what follows:

The Cavity Tuning Control Loop regulates the impedance angle of the cavity (represented as Z_{cav} in Fig. 1). Presently it derives its feedback from the RF phase between the RF power amplifier (PA) anode and cathode signals. For the remainder of this discussion, it is assumed that the Cavity Tuning Control Loop has been calibrated and is functioning normally.

The LLRF Beam Phase Locked Loop synchronizes the LLRF frequency with the beam revolution frequency. The LLRF Radial Position Loop regulates the beam energy by adjusting the LLRF output phase; thereby adjusting the beam synchronous phase angle.

Direct RF FB Loop & the Phase Unwrap Module

The Direct RF FB Loop is considered part of both the amplitude regulation system and the phase regulation system since its error signal is derived from the raw RF vector (amplitude and phase) difference between the RF drive signal and the cavity RF voltage fanback signal. Its role in the amplitude regulation system was previously discussed. Repeated here is a paragraph from that discussion which introduced its role in the phase regulation system:

> "The Direct RF FB zero error condition has to be satisfied in both magnitude and phase. In practice the phase is usually matched first by adjusting the phase unwrap delay line until the magnitude of v_{Error} is minimized. Then the magnitude is matched using a combination of β_{atten}, G_{OLG}, and v_{Drive}. The purpose of the phase unwrap module is to 'unwrap' the natural phase slope across the 300kHz frequency sweep that occurs due to the HLRF station's physical loop delay, essentially from v_{Drive} to v_{FB}."

The need for the phase unwrap module arises from the fact that the two RF signals which are being subtracted at the error summing junction are derived from different electrical path lengths. The first signal at Direct RF FB error summing junction is the RF setpoint which is derived from the RF drive signal, v_{Drive}, via a short path length on the Station RF Controller board through the amplifier G_{Set}. The second signal is the cavity RF voltage fanback signal, v_{FB}, which is also ultimately derived from v_{Drive}, but through a much longer path length: through the RF drive electronics in the gallery equipment racks, down to the cavity in the tunnel, and back up to the Station RF Controller in the gallery.

The difference in the path lengths (as determined from the phase unwrap delay line) is apparently ~425nsec. Thus, over the ~300kHz frequency sweep in the MI h588 system this equates to a phase change of ~46 degrees. Without the phase unwrap module, the phase of v_{FB} could be tuned via a cable length adjustment such that it is 180° out of phase with the v_{Drive} signal at the error summing junction; however, this adjustment would only work at a single frequency. At 300kHz away, the phase between the signals would be ~46° away from 180°.

It is the phase unwrap module that shifts the phase of v_{FB} automatically to effectively undo the phase change from the electrical path length difference. The present phase unwrap module accomplishes this phase shift through a process of down-converting the v_{FB} signal to an IF frequency and then up-converting it back to the RF operating frequency. The trick is that the LO (local oscillator) signal used for down-converting lags the LO signal used for up-converting by ~425nsec through the 'phase unwrap delay line'. Looking at it another way, the LO signal used for up-converting leads the LO signal used for down-converting. Since the LO signal is derived from the RF operating frequency, the LO signal is also experiencing a 300kHz frequency sweep. Thus, effectively, v_{FB} experiences a positive phase change in the phase unwrap module which cancels the negative phase change inherent in the physical path length difference. This process can be considered as an automatic phase shifter. The process isn't confined to the specific implementation that the phase unwrap module provides. Furthermore, although the path length appears to have been canceled through the phase shifting, causality is not violated; and the time delay of the system is still real and affecting the stability margins of the Direct RF FB loop.

The copied paragraph above only briefly mentions the first order calibration procedure of the Direct RF FB Loop. The process is usually an iterative one, but it does start best with adjusting the 'phase unwrap delay line' first while minimizing v_{Error} in open-loop (Direct RF FB off or I:RFFBG=0) on a spectrum analyzer in zero span mode with a 1MHz detection bandwidth to capture the frequency change of the h588 RF during the time duration of a cycle. Once v_{Error} is minimized with respect to the 'phase unwrap delay line' then the Direct RF FB magnitude adjustment is performed. Then the phase adjustment via the 'phase unwrap delay line' is repeated; but this time the local station phase error (with the 'Local Station Phase Control Loop' off) is monitored both with and without Direct RF FB applied. If the 'phase unwrap delay line' is tuned properly, there will be a minimal offset across the 300kHz frequency sweep between the two conditions. The noise in the local station phase error, however, should be much improved with Direct RF FB applied. The process of calibrating the Direct RF FB magnitude response can then be repeated if desired.

Local Station Phase Control Loop

The 'Local Station Phase Control Loop' is the next phase loop just outside of the Direct RF FB loop. It is composed of the 'Local Phase Shifter', the 'Local Phase Delay Line' and the 'Local Phase Detector' as shown in the main block diagram of Fig. 1. Before the Direct RF FB loop existed it was the only phase control loop at the local station level. In the presence of the Direct RF FB loop, which does help to improve the phase response, the 'Local Station Phase Control Loop' still is the ultimate control of the local station phase since it is the outermost loop at the station level. It compensates for imperfections in the Direct RF FB phase control and also for phase drifts in the system. It is a pure phase loop as opposed to the Direct RF FB loop which provides vector control. It can, of course, become coupled to the amplitude loops through the cavity impedance and interaction with the beam.

In order for all stations to effectively have the same electrical delay, the electrical delay of all the 'Local Phase Delay Lines' are made equal. The loop is tuned in open loop by adjusting the electrical delay inside the loop to closely match the electrical delay of the delay line. The match is measured using the 'Local Phase Detector'. Once the open loop response results in near zero phase (between the station's fanback signal and the delay line) across the 300kHz frequency sweep, then the loop is closed by activating the 'Local Phase Shifter' via its front panel control range knob.

Adjustments of station-to-station phase can then be made by adjusting the length of the RF fanout cabling to each station in front of the Local Station Phase Control at each station's RF equipment rack. The station-to-station phase is measured in the MI control room at the HLRF fanback module. The positions of the MI h588 cavities along the beam path in the tunnel are such that the phase between consecutive stations should be 180° at all frequencies across the frequency sweep. The only exception to this is between stations 9 and 10 which are further separated such that their relative phase between each other should be 0° (as if there is a station between them).

MRF Phase Control Loop

The MRF Phase Control Loop consists of two separate phase loops for Stage I: one for regulating the resultant phase of each group of 9 stations, Group A and Group B. An excerpt from the main block diagram that represents the MRF phase loop of a single group (i.e. Group A) is shown in Fig. 16.

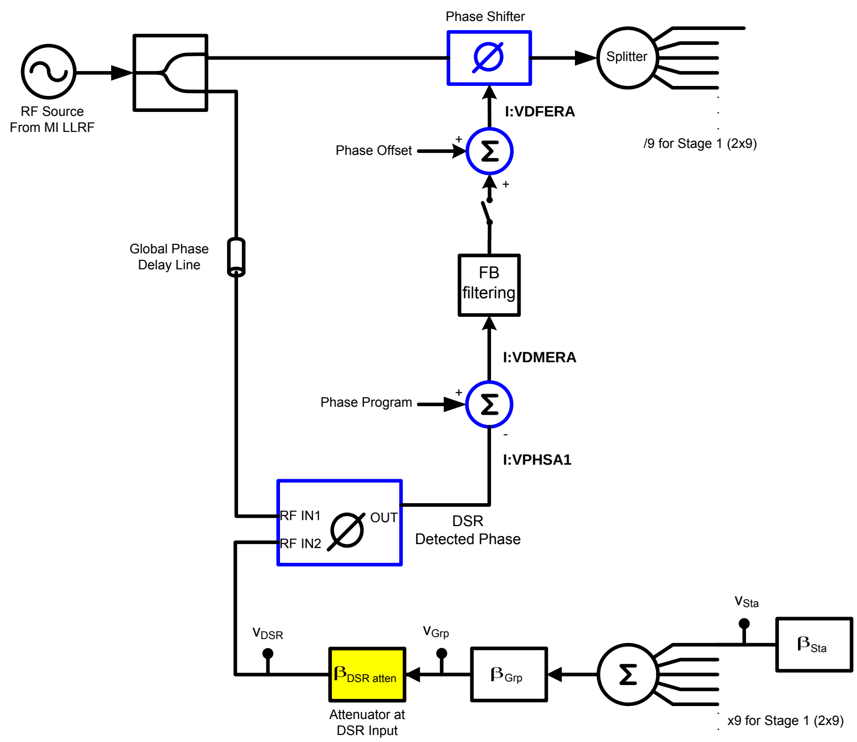


Figure 16: Simplified block diagram of the MRF phase loop of a single group, Group A

The phase between a reference signal and the group's vector sum, v_{DSR}, is detected by a Digital Signal Receiver (DSR) and compared to a 'Phase Program'. The 'Phase Program' is currently a static value, typically zero. The resultant phase error is amplified and filtered through a feedback filter (identical to the amplitude FB filter architecture shown on in Fig. 13 of p.32) before being applied as the phase shifting control signal to the MRF Direct Digital Synthesizer (DDS) (represented as the 'Phase Shifter' block). A 'Phase Offset' to the phase shifter control is included in order to calibrate out small phase errors in the system. More will be said on this shortly.

The reference signal used for the DSR phase detection is derived from the RF source through the 'Global Phase Delay Line'. There are a total of 2 global delay lines; one for each group. Each global phase delay line was tuned such that the DSR detected phase reads near zero with the MRF DDS's out of the system. This was done such that when the MRF is installed into the system it will minimally perturb the original phase of the HLRF system as it tries to regulate to zero. This was necessary in order not to greatly perturb the average phase of the HLRF system with respect to beam during the MRF upgrade.

A detailed diagram of the MRF phase control in the MRF DDS's is shown in Fig. 17.

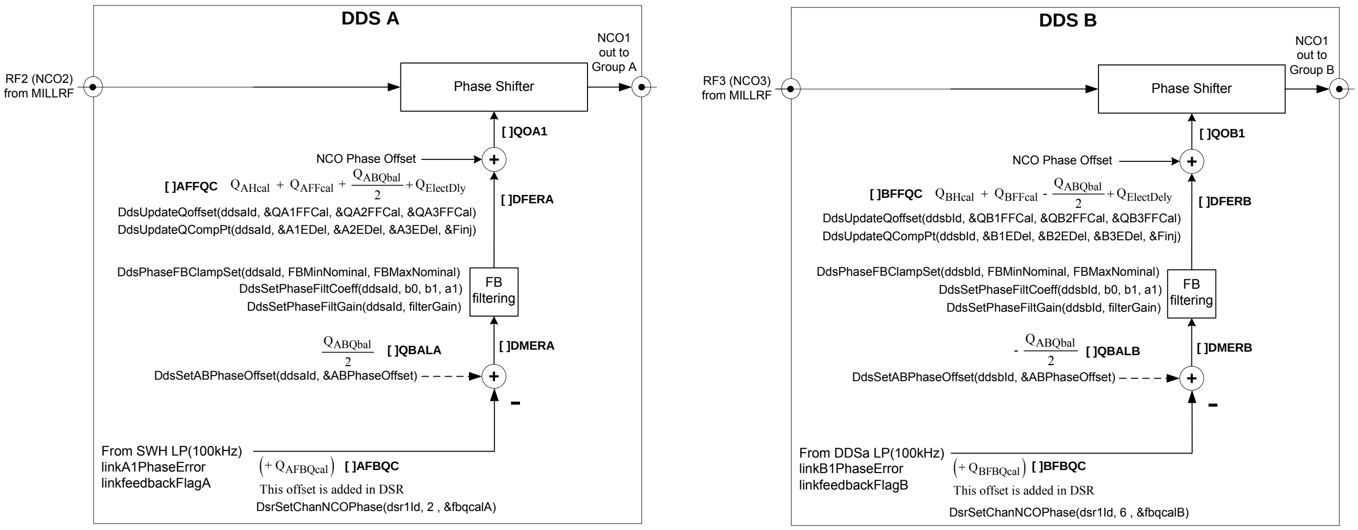


Figure 17: A more detailed diagram of the MRF phase control parameters in the MRF DDS's

The RF Source signals for the MRF DDS's originate from the MI low-level RF (LLRF) system's DDS's. For Group A, MI LLRF RF2 (NCO2) is the RF source. For Group B, MI LLRF RF3 (NCO3) is the RF source. The MRF DDS's are merely used as precision phase shifters. All of the original RF Source modulations needed for various MI h588 RF manipulations and the beam phase-locked-loop are still handled by the MI LLRF system. The MRF phase regulation system merely tries to force the resultant phase of each HLRF group to follow the phase of its LLRF source.

➢ *Calibration Parameters & the new A/B Phase Balance I:VQBAL*

Various calibration parameters were designed into the MRF phase control loop. These calibration parameters are shown in Fig. 17 as inputs to the 'NCO Phase Offset', as the set-point input of the phase error summing junction, and as an offset to the detected phase from the DSR. The intended use of these calibration parameters are for:

1) a calibration offset for the MRF DDS A(B) hardware via $Q_{A(B)Hcal}$,
2) a feed-forward correction term for small imperfections in the A(B) fanout system external to the MRF DDS's via $Q_{A(B)FFcal}$,
3) a calibration of the DSR A/(B) fan-back detected phase via $Q_{A(B)FBQcal}$ to compensate for small imperfections in the fan-back system,
4) a calibration term for the phase balance between group A and B via Q_{ABQbal} ; intended for use with para-phasing
5) nulling out the electrical delay added to the original system by the MRF DDS and associated cabling via $Q_{ElectDly}$.

Items 1-3 are self-explanatory. Item 4 represents a new A/B Phase Balance feature that the MRF provides which may be useful for para-phasing. Para-phasing is a term used to describe the process by which the Group A and B vectors are rotated out-of-phase from each other to produce a lower sum voltage. The MI LLRF system, as mentioned previously, provides the para-phasing control. However, since the MRF DDS's are in the forward path, they can provide a simple phase offset between Group A and B for fine tuning control aside from the fast waveform arrays that are already used in the MI LLRF system.

As seen in Fig. 17, ½ of the adjustable A/B phase balance parameter, Q_{ABQbal} , is added to the phase program set-point at the phase error summing junction in MRF DDS A, while the same amount is subtracted from the set-point in MRF DDS B. Thus the adjustable phase balance parameter is split between the two vectors. By adding the offset to the set-point, the MRF phase regulation loop will try to regulate to this offset when reducing the phase error (set-point – detected phase) to zero. In order to help the phase loop achieve this zero error, a phase 'drive' term equal to the A/B balance set-point is added to the 'NCO Phase Offset' of each DDS. Thus, the +/- ½ of Q_{ABQbal} also appears in the 'NCO Phase Offset' term represented as []A(B)FFQC in each DDS. Thus the structure for the phase balance term is similar to a 'drive + error' control system. Q_{ABQbal} is adjustable via ACNET device I:VQBAL.

Finally, item 5 in the list of phase calibration parameters deserves a brief explanation. Since the MRF DDS's and associated cabling add electrical delay to the system when installed, it was necessary to compensate for this added electrical delay in order to minimize the impact on operations (as discussed previously). A software negative electrical delay line was added to each MRF DDS' 'NCO Phase Offset' program. The amount of electrical delay compensated for during the MRF development and studies was 113.612 nsec.

New I6 Sequence Table Messages & h588 Curves

The following new messages have been made available on I6 for MRF use:

- V588 Feedback – for turning MRF feedback on/off and setting FB gains
- V588Set – for abruptly setting the h588 request voltage and number of stations
- V588Play – for adiabatically changing the h588 request voltage
- V588APG(t)Curve – for returning to the APG curve (i.e. from a set or play message)

For a detailed description of these new messages, see the I6 on-line help.

Another feature added to I6 is the addition of HLRF curves to I6. Currently, there are two additional sets of HLRF curves: Expert1, and Expert2. The expert curves can be tuned on I6 and are accessible under the 'Curves' drop down menu at the top of I6. In particular the path to Expert1 and Expert2 curves are respectively Curves/HLRF/MRF/0 and Curves/HLRF/MRF/1. Both sets include all the standard I3 front end curves (I:RFAPG, I:FFAMP, etc. – both time and momentum where applicable).

In the 'required data' on I6, each MI state sequence table can choose whether the MRF front end curves originate from either the I3 Curves, Expert1, or Expert2 curve sets. The I3 Curves is the default choice which uses the standard I3 operational set of curves. The choice is an 'expert only' selection available in the 'h588 Curves' section of the 'required data'. Currently these expert curve sets are useful for system calibrations. However, it is hoped that one day the number of curve sets can be increased in order to achieve true MI state control of the front end curves; i.e. a curve set for each MI state instead of only the 8 presently Tclk mapped curve sets.

References

[1] T. Berenc, B.Chase, "Status of the Main Injector Mid-Level Radio Frequency (MRF) Project- a Run II Main Injector Upgrade", Fermilab RF TechNote #069, http://www-rfes.fnal.gov/global/technotes/TN/TN069.pdf

[2] T.Berenc, "Main Injector HLRF Station Gain Measurements", Fermilab RF TechNote #070, http://www-rfes.fnal.gov/global/technotes/TN/TN070.pdf

[3] T.Berenc, B.Chase, P.Joireman, P.Varghese, "Main Injector HLRF ON/OFF and Track/Hold Gates Timing", Fermilab RF TechNote #072, http://www-rfes.fnal.gov/global/technotes/TN/TN072.pdf

[4] T.Berenc, B.Chase, R.Pasquinelli, J.Reid, "A Brief History of the MI 53MHz RF System Run II Upgrades", Fermilab RF TechNote #073, http://www-rfes.fnal.gov/global/technotes/TN/TN073.pdf

Appendix

Direct RF FB Scaling Factors

for both the MI-60 Test Station and the MRF operational system

	Test Station (DSR GrpA)		***Grp A MRF_Oper***		***Grp B MRF_Oper***	
Factor	**dB**	**lin Mag**	**dB**	**lin Mag**	**dB**	**lin Mag**
β_{mon}	-100	1.0E-05	-100	1.0E-05	-100	1.0E-05
$\beta_{US\ cable}$	-7.66	0.414	-7.32	0.431	-7.32	0.431
β_{FB}	-107.66	4.14E-06	-107.32	4.31E-06	-107.32	4.31E-06
β_{atten}	-5	0.562	-5	0.562	-5	0.562
β_{unwrap}	10.83	3.479	10.83	3.479	10.83	3.479
$v_{Gap} / v_{Gap\ Mon}$	107.66	2.42E+05	107.32	2.32E+05	107.32	2.32E+05
v_{Gap} / v_{FB}	101.83	1.23E+05	101.49	1.19E+05	101.49	1.19E+05

$$\beta_{FB} = \beta_{mon} \cdot \beta_{US\ cable}$$

$$\frac{v_{Gap}}{v_{Gap\ Mon}} = \frac{1}{\beta_{FB}} \qquad \frac{v_{Gap}}{v_{FB}} = \frac{1}{\beta_{FB} \cdot \beta_{atten} \cdot \beta_{unwrap}}$$

Notes:

1. The β_{atten} value shown above was determined during the VGA upgrade installation as a compromise of the Direct RF FB error at injection and flat top during a MI State 05, Tclk 23 cycle which used Grid Bias Offset programming at the beginning of the cycle and without any RFOLG tuning. The actual value at each station may vary and will be dictated by a thorough system calibration.
2. The MRF mode (Test Station or Operational) can be controlled via ACNET device I:VMRFVM. See LLRF documentation for details.

MRF Amplitude Feedback Scaling Factors
for both the MI-60 Test Station and the MRF operational system

Factor	Test Station (DSR GrpA) dB	Test Station (DSR GrpA) lin Mag	Grp A MRF_Oper dB	Grp A MRF_Oper lin Mag	Grp B MRF_Oper dB	Grp B MRF_Oper lin Mag
β_{Mon}	-100	1.00E-05	-100	1.00E-05	-100	1.00E-05
$\beta_{DS\ cable}$	-4	0.631	-4	0.631	-4	0.631
$\beta_{FanBack\ cable}$	-1.27	0.864	-1.1	0.881	-1.1	0.881
$\beta_{FanBack\ chassis}$	0	1	-19.16	0.110	-18.55	0.118
$\beta_{DSR\ cable}$	-0.3	0.966	-0.3	0.966	-0.3	0.966

β_{Sta}	-105.27	5.45E-06	-105.1	5.56E-06	-105.1	5.56E-06
β_{Grp}	-0.3	0.966	-19.46	0.106	-18.85	0.114
$\beta_{DSR\ atten}$	-20.0	0.100	-2	0.794328	-2	0.794328
v_{Gap} / v_{DSR}	125.57	1.90E+06	126.56	2.13E+06	125.95	1.98E+06
$v_{max\ DSR}$ (Vpk)		2.2		1.1		1.1
$v_{meas\ max}$ (Vpk)		4.18E+06		2.34E+06		2.18E+06

$\beta_{DSR\ IQ}$	143.0	1.42E+07	143.0	1.42E+07	143.1	1.43E+07
$\beta_{DSR\ Pot}$	-17.5	0.1338	-16.5	0.15017	-17.2	0.13863
$v_{Gap} / v_{Grp\ Meas}$	0.00	1.00	-0.02	1.00	0.01	1.00

$$\beta_{Sta} = \beta_{mon} \cdot \beta_{DS\ cable} \cdot \beta_{FanBack\ cable} \qquad \beta_{Grp} = \beta_{FanBack\ chassis} \cdot \beta_{DSR\ cable}$$

$$\frac{v_{Gap}}{v_{DSR}} = \frac{1}{\beta_{Sta} \cdot \beta_{Grp} \cdot \beta_{DSR\ atten}} \qquad \frac{v_{Gap}}{v_{Grp}} = \frac{1}{\beta_{Sta} \cdot \beta_{Grp}}$$

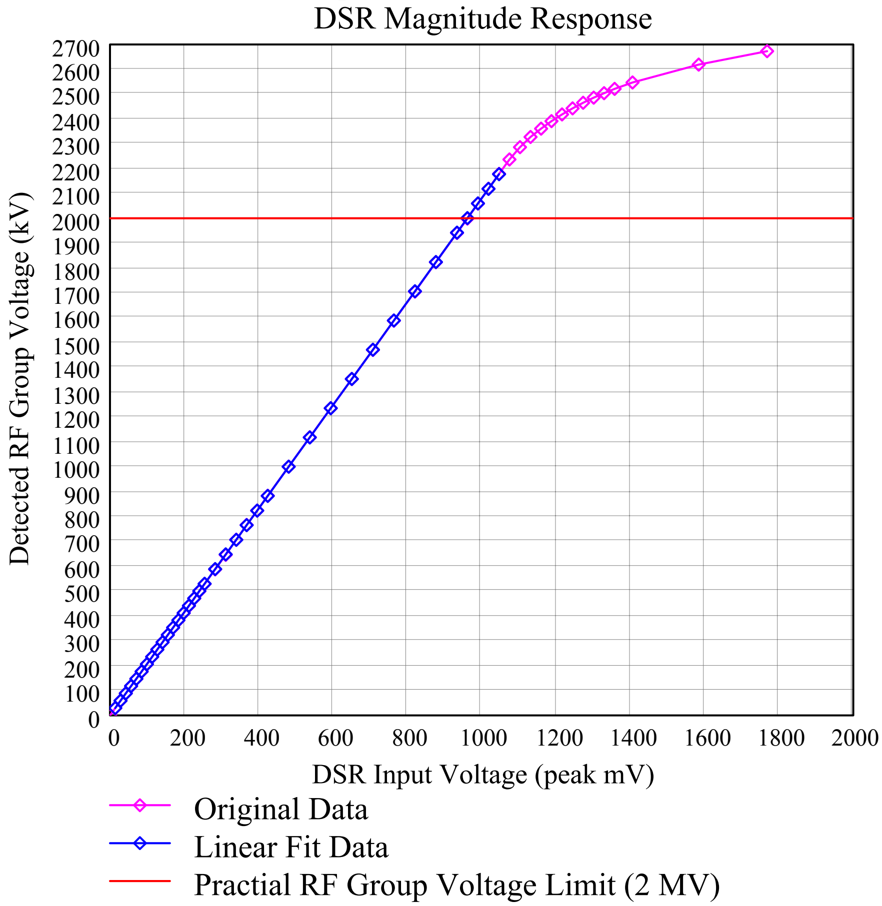
$$\frac{v_{Gap}}{v_{Grp\ Meas}} = \frac{1}{\beta_{Sta} \cdot \beta_{Grp} \cdot \beta_{DSR\ atten} \cdot \beta_{DSR\ IQ} \cdot \beta_{DSR\ Pot}}$$

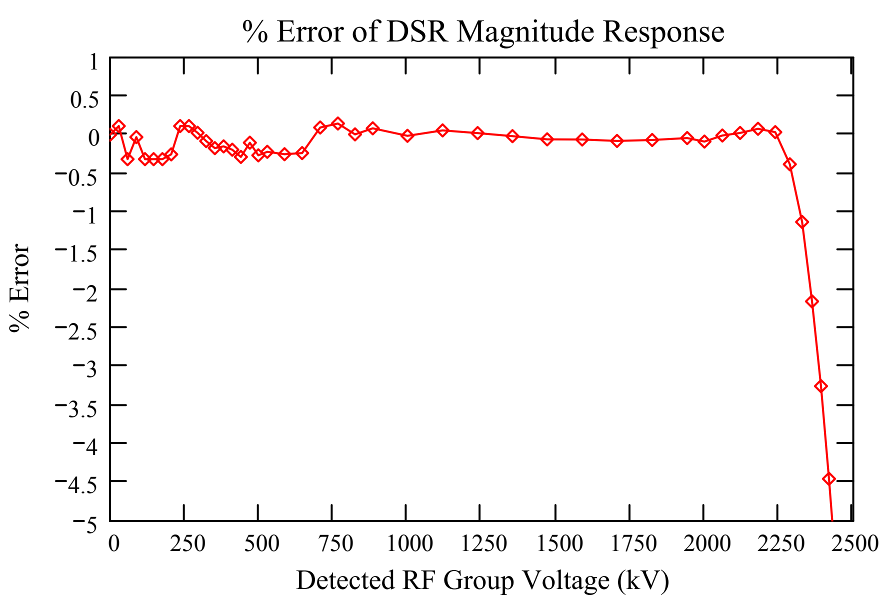
Notes:

1. The fanback chassis values $\beta_{FanBack\ chassis}$ above are not measured values but were inferred from the other values and the $\beta_{DSR\ Pot}$ values used during MRF development studies.
2. To increase the maximum measurable signal, $v_{meas\ \max}$ (which is dictated by the maximum DSR input signal $v_{\max\ DSR}$), increase the DSR input attenuator, $\beta_{DSR\ atten}$. Then to maintain a unity scaling for $\frac{v_{Gap}}{v_{Grp\ Meas}}$ adjust the A/B pots ($\beta_{DSR\ Pot}$ above) via ACNET devices I:VAPOT and I:VBPOT.
3. The values above were determined during MRF development. They have not yet been confirmed via a thorough beam based calibration method. For actual operational A/B pot values see ACNET devices I:VAPOT and I:VBPOT.

Typical MRF DSR Magnitude Response

This data was taken on the MRF Development system Group A input channel. It assumes that the APOT value was equal to 0.1372.





MRF Front End Curves Scalings

I3 Curve				XFR ftp Variables				XFR Output	
Curve	*primary unit*	*common xform*	*common units*	*ACNET device*	*primary unit*	*common xform*	*common units*	*Scaling*	*Output Units*
I:FFAMP	Volt	X'=X	Unit	**I:VFFAMP**	Volt	X'=X	Volt	1	
I:RFAPG	MV	X'=X	MV	**I:VAPGT**	MV	X'=X	MV	1000	kV
I:RFALP	Volt	X'=27.5625*X-12.25	kV	**I:VALP**	Volt	X'=27.5625*X-12.25	kV	X'=27.5625*X-12.25	kV
I:RFBPG	Volt	X'=250*X	Amp	**I:VBPG**	Volt	X'=250*X	Amp	1	Volt
I:RFCQG	Volt	X'=X	Unit	**I:VCQG**	Volt	X'=X	Volt	1	Volt
I:RFOLG	Volt	X'=(1+X/7.5)*100	%	**I:VOLG**	Volt	X'=(1+X/7.5)*100	%	1	Volt
I:RFGBP	Volt	X'=50*X	Volt	**I:VGBP**	Volt	X'=50*X	Volt	1	Volt
I:RFFBG	Volt	see Note (1)	V/V	**I:VFBG**	Volt	see Note (1)	V/V	1	Volt

Notes:

(1) See the 'Direct RF FB Gain' discussion for the ACNET device common transform used for the Direct RF FB gain.

Definitions:

Primary units:

units used as a practical measurement of a system parameter and used to determine the actual quantity of common (engineering) units of that parameter. Most commonly the primary units are volts since most devices in the system are voltage controlled and most sensors produce a voltage proportional to a system parameter.

Common (Engineering) units:

The natural physical units used to describe the parameters of a system (i.e. kV for gap voltage, Amps for current).

MRF SWH ACNET Devices

ACNET device Name	Description	primary unit	common xform	common units	SWH Station Scaling		Notes
					Parameter Gain	Parameter Offset	
I:VSAPGI	APG curve in MRF SWH	kV	X' = X/1000	MV	N/A	N/A	APG(t) curve in front of the fader in MRF SWH
I:VV53R	MRF h588 Vrequest	kV	X' = X/1000	MV	N/A	N/A	The requested h588 Sum Voltage assuming there is no counter-phasing between Group A and B.
I:VSMAGA	Grp-A Det Magnitude	kV	X' = X	kV	N/A	N/A	The Group A(/B) detected cavity sum volt. magnitude
I:VSMAGB	Grp-B Det Magnitude	kV	X' = X	kV	N/A	N/A	
I:VSMERA	SWH GrpA Mag Error	kV	X' = X	kV	N/A	N/A	The MRF group A(/B) magnitude error.
I:VSMERB	SWH GrpB Mag Error	kV	X' = X	kV	N/A	N/A	
I:VSPERA	GrpA Mag SetPlusErr	kV	X' = X	kV	N/A	N/A	The MRF magnitude setpoint plus error summing junction output in group A(/B) sum voltage.
I:VSPERB	GrpB Mag SetPlusErr	kV	X' = X	kV	N/A	N/A	
I:VSSSDA	GrpA Sta SSD in SWH	kV	X' = X	kV	24.444	0	The cavity gap voltage request for each station in kV.
I:VSSSDB	GrpB Sta SSD in SWH	kV	X' = X	kV	24.444	0	
I:VSAPGA	GrpA Sta APG in SWH	kV	X' = (X/12.25)+1.00	kV	27.5625	12.25	Primary units are cavity gap voltage request in kV for each station while common units are station Modulator output voltage in kV assuming a station APG prg. adjust module scaling factor of 0.75 and a gap to anode ratio of 12.25.
I:VSAPGB	GrpB Sta APG in SWH	kV	X' = (X/12.25)+1.00	kV	27.5625	12.25	
I:VSFAMP	FFAMP in MRF SWH	V	X' = X	V	1	0	see Feed-Forward BLC system experts for details
I:VSBPG	BPG in MRF SWH	V	X' = 250*X	Amps	1	0	Common units are Bias Supply output current.
I:VSOLG	OLG in MRF SWH	V	X' = (1+X / 7.5)*100	%	1	5	The +5 parameter offset is needed since this MRF DAC channel is bipolar and expects a 0-10 input. The I3 program should be tuned bipolar from -5v to +5v.
I:VSGBP	GBP in MRF SWH	V	X' = 50*X	V	1	0	Primary units are DAC output volts while common units are in actual Grid Bias offset Volts assuming unity scaling at the station Grid Bias offset program adjust module.
I:VSFBG	FBG in MRF SWH	V	see the 'Direct RF FB Gain' discussion	V/V	1	0	Primary units are DAC output volts while common units are closed loop voltage Gain in linear units.
I:VAPOT	Grp A Mag scale adjust	N/A	N/A	N/A	N/A	N/A	The group A(/B) detected magnitude scaling adjustment for fine tuning. Equivalent to the 'A/B Pots'.
I:VBPOT	Grp B Mag scale adjust	N/A	N/A	N/A	N/A	N/A	

MRF DSR & DDS ACNET Devices

ACNET device Name	*Description*	*primary unit*	*common xform*	*common units*	*Notes*
I:VPHSA1	GrpA DSR Det Phase	deg	X' = X	deg	The detected phase calibration offset I:A(/B)FBQC is included in this measurement.
I:VPHSB1	GrpB DSR Det Phase	deg	X' = X	deg	
I:VDMERA	GrpA phase error	deg	X' = X	deg	located in DDSA(/B)
I:VDMERB	GrpB phase error	deg	X' = X	deg	
I:VDFERA	GrpA phs error filter out	deg	X' = X	deg	The DDSA(/B) phase error feedback filter output
I:VDFERB	GrpB phs error filter out	deg	X' = X	deg	
I:AFFQC	GrpA feed fwd phase cal	deg	X' = X	deg	The sum of the feed forward phase calibration terms including the DDS hardware, the fanout system, and the A/B phase balance terms
I:BFFQC	GrpB feed fwd phase cal	deg	X' = X	deg	
I:AFBQC	GrpA DSR phase cal offset	deg	X' = X	deg	The phase offset calibration in the DSR intended for compensating for the fanback system.
I:BFBQC	GrpB DSR phase cal offset	deg	X' = X	deg	
I:QBALA	GrpA A/B phase cal	deg	X' = X	deg	The A(/B) phase setpoint for the A(/B) phase regulation loop. Presently this is just the A/B phase balance term.
I:QBALB	GrpB A/B phase cal	deg	X' = X	deg	
I:QOA1	GrpA phs shifter control	deg	X' = X	deg	The A(/B) DDS phase shifter control signal. It is the sum of I:VDFERA(/B) and the phase calibration terms.
I:QOB1	GrpB phs shifter control	deg	X' = X	deg	