

Gating System for Recycler 1.75 GHz Schottky Detector

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Abstract

The gating system for the Recycler 1.75 GHz schottky detector is presented in this paper. The gating circuit and its operation is described, along with the ACNET programming. The complete schottky system is described in [1].

Gating System

A simplified block diagram of the gating system is shown in fig. 1. The schottky signal is split into three signals at the input to the circuit. Two of the signals are gated and one signal is a reference signal. The gating of the signals is done with a double-balanced mixer for best isolation. The input signal goes into the LO port of the mixer, the output goes out the RF port, and the ON/OFF gating signal is applied to the IF port. A VME crate located in MI60 provides a TTL ON/OFF gating signal with the gate ON being TTL high, and the gate OFF being TTL low. There are a total of eight schottky signals; horizontal proton sum, horizontal proton delta, horizontal pbar sum, horizontal pbar delta, vertical proton sum, vertical proton delta, vertical pbar sum, and vertical pbar delta. The gating circuit shown in fig. 1 is applied to each of these signals.

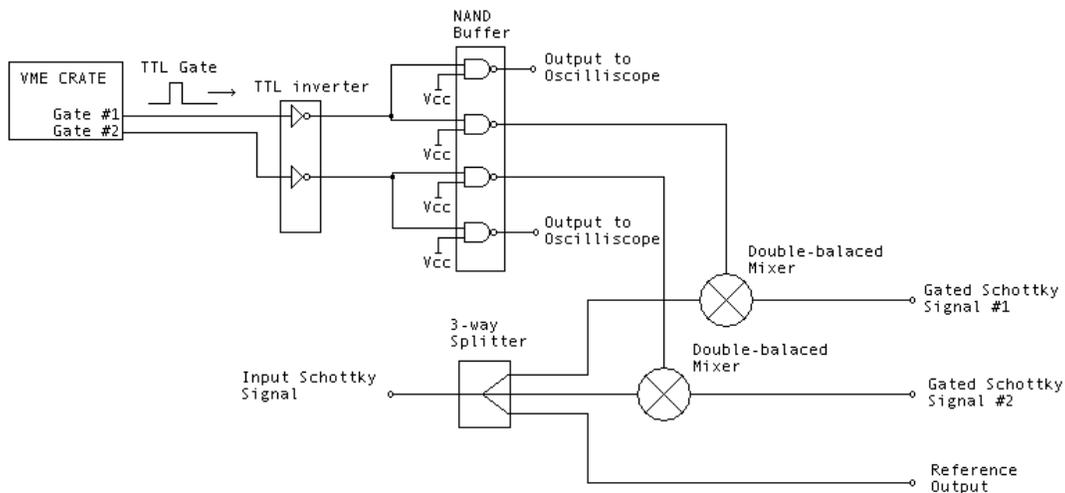


Fig. 1. Schottky gating block diagram

Gating Circuit Card

One circuit card is used for two of the schottky signals (the SUM and the DELTA). There are a total of four circuit cards; one for the proton horizontal signals, one for the proton vertical signals, one for the pbar horizontal signals, and one for the pbar vertical signals. A circuit schematic of the circuit card is shown in fig. 2. The drawing number for the circuit schematic is #0880.00-EC-417022. Two circuit cards are housed in a 19 inch chassis, for a total of two chassis's for the system. One chassis houses the horizontal circuit cards, and one chassis houses the vertical circuit cards. The drawing number for the chassis's is #0880.00-LB-417012.

It is desired that the TTL gating signal be buffered before it goes to the mixer because of the 50 Ohm impedance at the IF port, so a driver circuit is used. The driver circuit selected is the 74f3037 NAND 30 Ohm driver. This is a stock item and it provides more than enough power to drive the 50 Ohm input at the IF port of the mixer. Since the circuit is a NAND gate, an inverter is needed to keep the polarity of the ON/OFF signal correct. There is also circuitry to bring the ground pins of the NAND buffer to a negative voltage. This brings the TTL LOW voltage to exactly zero volts, so that the gate mixer will be completely OFF when the gate signal is LOW. A potentiometer, located on the front panel of the chassis that the circuit cards are located in, is used to make this adjustment. The circuit also buffers an extra gate signals so that the gate levels and timing can be looked at on a scope.

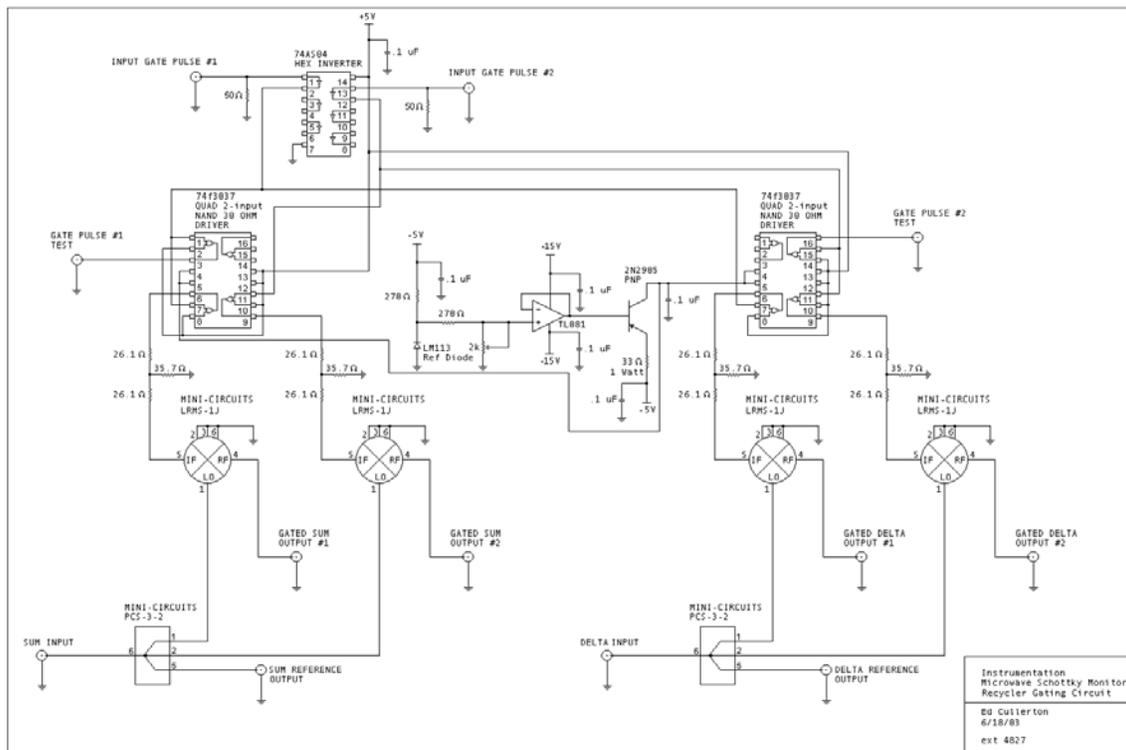


Fig. 2. Gating circuit card schematic

ACNET Gate Signal

A VME crate in MI-60 generates the TTL gate signal, which is ACNET programmable. The timing of the gates is programmable using the MDAT beam marker as a reference point to turn ON and turn OFF the gates. The MDAT leading edge and trailing edge is set by R:SCGHO and R:SCGLO. Setting these values to 0084 and 0085 triggers the MDAT leading and trailing edges to the injected beam. A setting of 0080 and 0081 triggers the MDAT leading and trailing edges to cooled beam. The bucket position of the MDAT leading and trailing edges are displayed by R:SCHMDT and R:SCLMDT. R:SCHBKT is the gate #1 start position, in number of buckets delayed from the MDAT leading edge marker, and R:SCLBKT is the gate #1 stop position, in number of buckets delayed from the MDAT trailing edge marker. Gate #2 is programmed in the same fashion with R:SCHBK1 and R:SCLBK1.

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PA:R34 INSTRUMENT PARAMS
R34 RCYL SCHOTTKY TIMING GATE MI60SET D/A A/D Com-U PTools
-<FTP>+ *SA X-A/D X=TIME Y=I:RFAPGF,I:FFAMPF,I:MMNTUM,T ERING
COMMAND BL-- Volts I= 0 I= 0 , 0 , 0 , 0
-< 3>+ s_MI AUTO F= .4 F= 10 , 4 , 40 , 1000
toroid FLUX... rad_mon dclt... bpm_nod ipm... peanuts testdev
! ENABLE BSYC, MDAT, TCLK
! FREE RUN OFF: GATE(S) AFTER TCLOCK EVENT
! FREE RUN ON: CONTINUOUS GATE ON EVERY TURN
R:SCBSYC RR SchottkyGate BSYC Ena ..
R:SCTCLK RR Schottky Gate TCLKE na *
R:SCMDAT RR SchottkyGate MDAT Ena .
R:SCFRUN RR SchottkyGate FreeRnEn .

! SET TURN MARKER TO C0 (CZERO)
-R:SCTMKR RR Schottky Turn Marker 00C0 00C0
-R:SCSKIP RR SchottkyGate SkipSmpl 0 0 Turn
-R:SCHBKT RR SchottkyGate On Delay 0 0 Bkts
-R:SCLBKT RR SchottkyGateOff Delay 485 485 Bkts
-R:SCHBK1 RR SchottkyGate On Delay 0 0 Bkts
-R:SCLBK1 RR SchottkyGateOff Delay 0 0 Bkts

! CHOOSE BARRIERS ASSOCIATED WITH GATE EDGE
-R:SCGHO RR SchotkyGateOn MDAType 0084 0084
-R:SCGLO RR SchtkyGateOff MDAType 0085 0085
R:SCHMDT RR SchottkyGateOff MDAT 576 Bkts
R:SCLMDT RR SchottkyGateOff MDAT 121 Bkts

! IF FREE RUN DISABLED: SELECTS BURST COUNT,
! DELAY, TCLOCK TRIGGER EVENT
-R:SCCNT RR SchottkyGate #Samples 0 0 Cnts
-R:SCTDLY RR SchottkyGate TCLK 0 0 Secs
-R:SCEVNT RR SchtkyGate ArmTCLKEvt 00FF 00FF */
-R:SCECNT RR SchtkyGat #TCLKTriggr 1 1 Cnts

-R:MDAT80 Recycler MDAT Xmit Ch 0 287 376 BKTS
-R:MDAT81 Recycler MDAT Xmit Ch 1 297 528 BKTS
-R:MDAT82 Recycler MDAT Xmit Ch 2 307 169 BKTS
-R:MDAT83 Recycler MDAT Xmit Ch 3 317 328 BKTS
-R:MDAT84 Recycler MDAT Xmit Ch 4 327 576 BKTS
-R:MDAT85 Recycler MDAT Xmit Ch 5 337 121 BKTS

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Fig. 3. ACNET parameter page for control the gate timing

The actual position of the two gates can be compared to the beam using an oscilloscope. The oscilloscope is programmable using the web page <http://rec-gate-scope.fnal.gov>. The web page is shown in fig. 4. Channel one is gate one, channel two is gate two, channel three is any one of the ungated reference signals multiplexed in from R41, and channel four is any one of the gated signals multiplexed in from R74. It is critical that the cable lengths are the same going to the oscilloscope so that the beam reference signals and the gates are timed correctly. The gates displayed on channels 1 and 2 of the scope are hard wired in from the vertical proton gate buffers and display only the gates that are applied to the vertical proton schottky signals. These gates are identical to the gates on all the other schottky signals, so it is not necessary to multiplex each gate into the oscilloscope. The scope is triggered using a MDAT signal coming from the same VME crate that supplies the gates. The scope is also displayed on channel 25 of the main injector television system. A photograph of the electronics is shown in fig. 5.

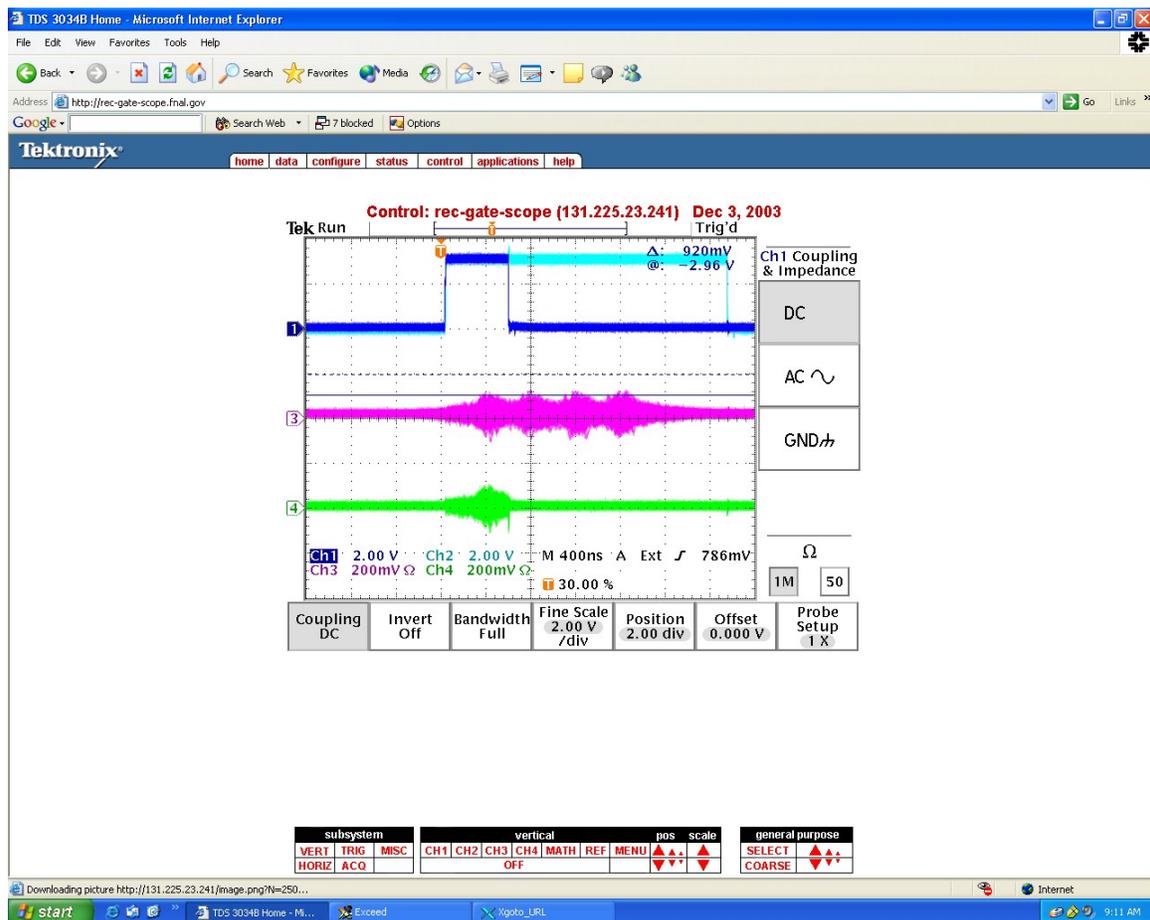


Fig. 4. Oscilloscope used for gate timing

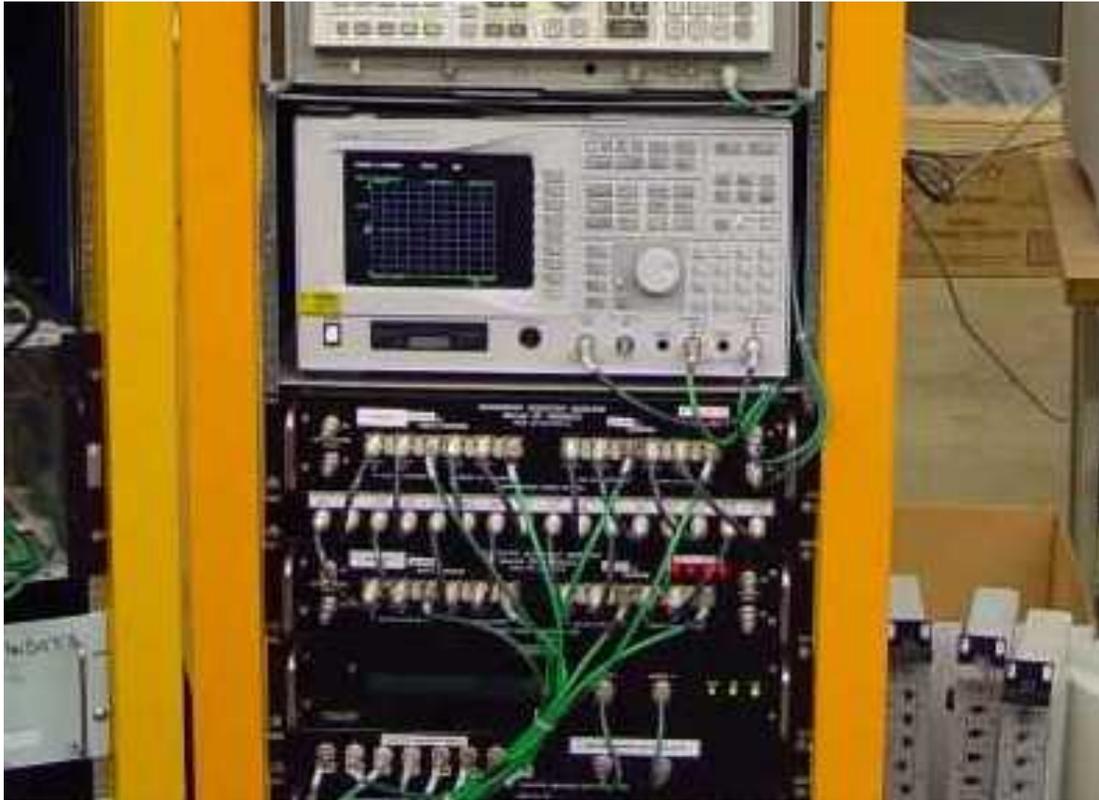


Fig. 5. Photograph of the installed electronics

[1] E. Cullerton, R. Pasquinelli, "A 1.75 GHz Waveguide Schottky Detector for the Recycler," Fermilab RF Department Note 63.