

Microwave Equalizer for the Antiproton Source 4-8 GHz Accumulator System

Ed Cullerton
Beams Division / RF & Instrumentation

Abstract: *A microwave equalizer for the antiproton source 4-8 GHz accumulator system is presented in this paper. The equalizer is designed to increase the overall cooling bandwidth of the system. The equalizer is fabricated in microstrip form and consists of 3 microstrip stubs with resistive terminations. The design procedure, simulated results, and measured results of the equalizer are presented in this paper.*

Design Considerations

The first step is to realize the limitations of the equalizer that will be fabricated. The equalizer is in microstrip form, and is fabricated using an etching machine. The dielectric material used is Arlon 31 mil, 2.33 dielectric constant. The length and width of each microstrip line must be considered when designing the equalizer. The lower limit for line width, using an etching machine, is about 10–15 mils. The lower and upper limit on the length of the microstrip stubs is about 100 mils and 1000 mils, respectively. This length limit is not absolute, but simulated and measured results have good agreement in this range. The equalizer simulations are done using HP ADS. Other constraints on the equalizer are insertion loss and return loss. The maximum insertion loss for this equalizer is 15 dB. The return loss at the input and output are designed to be better than –7 dB.

Design of the Equalizer

The transfer function of the accumulator system with beam is placed in a .s2p file. Only s21 data of the system is provided, and the other s-parameters are zero. The ADS schematic window is shown in fig 1. This schematic contains the s-parameter file of the data to be equalized, an amplifier to bring the peak of the data to zero, and a 180 phase shift element to bring the phase to zero. The 180 phase shift element is added only for simulation purposes, and to clearly view the phase. The normal operation of the accumulator requires the phase to be at 180 degrees for cooling. The data is from the accumulator horizontal lower side band. The data is shown in fig 2. This data serves as a reference for the design of the equalizer. Using this data, the frequency range of the equalizer is determined, and the –10 dB points are used to find the frequency range of the equalizer. This leaves about 5 dB of play for the equalizer, and a total insertion loss of –15 dB. The frequency range chosen is 3.7 GHz – 5.0 GHz.

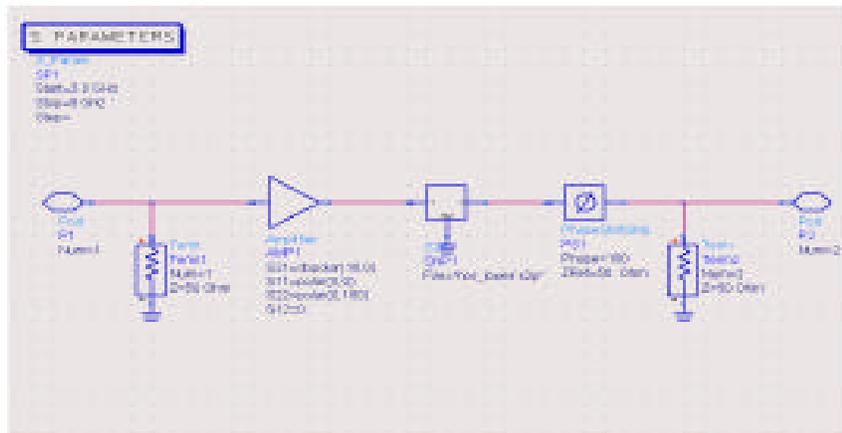


Fig. 1. ADS schematic used to display the transfer function of the accumulator system

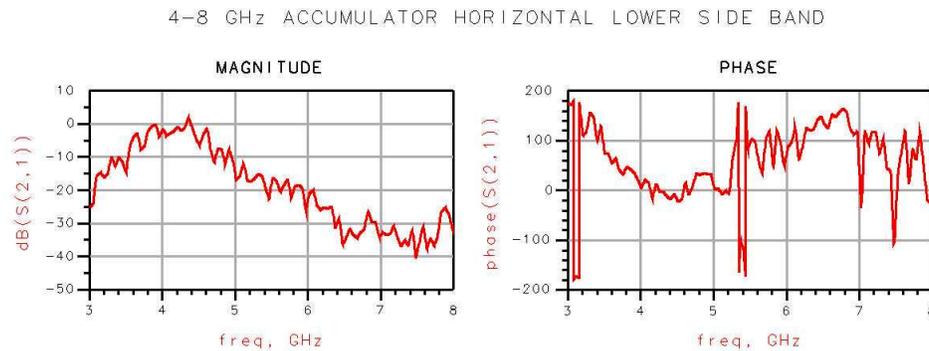


Fig. 2. Accumulator transfer function

The ADS schematic of the equalizer in series with the transfer function data is shown in fig 3. The optimizer in ADS is used in this design. To use the optimizer, the simulation elements must be set. Fig 4 shows the elements that are required to use the optimizer. The NOMINAL OPTIMIZATION element controls which goals are to be used, the type of optimization routine, and the number of iterations. For this equalizer, the GRADIENT optimization routine is used. The GOAL element defines which variable to optimize, and defines the desired value of the variable. For this equalizer, there are four goals. The goals are to flatten the magnitude, flatten the phase, and keep the return loss at the input and output to a minimum. The magnitude is set to a range of +/- 3dB, the phase is set to +/- 15 degrees, and the return loss is set to be better than -7 dB. Since the desired phase is 180 degrees, a 180 phase shift element is added to the schematic. The 180 phase shift makes it easier to view the results. Each goal is specified in the 3.9 – 4.8 GHz range. The range is slightly smaller than the 3.7 – 5.0 GHz range that was first decided, but a smaller range helps the optimizer to converge on a solution faster. The range can then be increased after the optimizer converges to the smaller frequency range. The magnitude goal is weighted higher so that the optimizer puts more emphasis on flattening the magnitude.

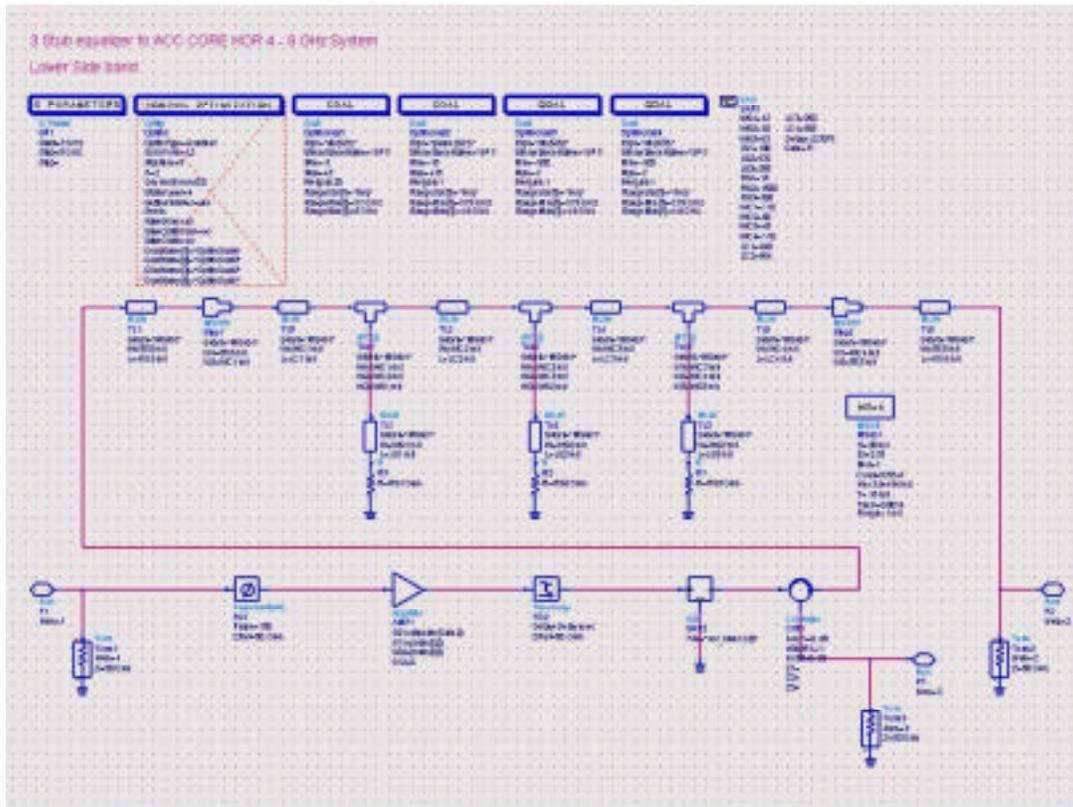


Fig. 3. ADS schematic of the equalizer

NOMINAL OPTIMIZATION.	GOAL	GOAL	GOAL	GOAL
Optim	Goal	Goal	Goal	Goal
Optim1	OptimGoal1	OptimGoal2	OptimGoal3	OptimGoal4
OptimType=Gradient	Expr="db(S21)"	Expr="phase(S21)"	Expr="db(S22)"	Expr="db(S33)"
ErrorForm=L2	SimInstanceName="SP1"	SimInstanceName="SP1"	SimInstanceName="SP1"	SimInstanceName="SP1"
MaxIters=15	Min=-3	Min=-15	Min=-100	Min=-100
P=2	Max=+3	Max=+15	Max=-7	Max=-7
DesiredError=0.0	Weight=20	Weight=1	Weight=1	Weight=1
StatusLevel=4	RangeVar[1]="freq"	RangeVar[1]="freq"	RangeVar[1]="freq"	RangeVar[1]="freq"
SetBestValues=yes	RangeMin[1]=3.9 GHz	RangeMin[1]=3.9 GHz	RangeMin[1]=3.9 GHz	RangeMin[1]=3.9 GHz
Seed=	RangeMax[1]=4.8 GHz	RangeMax[1]=4.8 GHz	RangeMax[1]=4.8 GHz	RangeMax[1]=4.8 GHz
SaveSols=no				
SaveOptimVars=no				
SaveGoals=no				
GoalName[1]="OptimGoal4"				
GoalName[2]="OptimGoal3"				
GoalName[3]="OptimGoal2"				
GoalName[4]="OptimGoal1"				

Fig. 4. Optimization elements in ADS.

The equalizer is composed of microstrip elements that have optimizable variables. The variable list is shown in fig 5. The variables are set to a midpoint between the maximum and minimum values to start. The variables are the length and width of each microstrip element, the value of resistors on the stubs, the gain to compensate for the insertion loss, and a delay to flatten the phase. The diagram in fig 6 shows the variables and their corresponding elements.

```

VAR
VAR1
WS1=89 opt{ 15 to 110 }
WS2=89 opt{ 15 to 110 }
WS3=89 opt{ 15 to 110 }
LS1=400 opt{ 100 to 1000 }
LS2=400 opt{ 100 to 1000 }
LS3=400 opt{ 100 to 1000 }
RS1=100 opt{ 0 to 5000 }
RS2=100 opt{ 0 to 5000 }
RS3=100 opt{ 0 to 5000 }
WC1=89 opt{ 15 to 110 }
WC2=89 opt{ 15 to 110 }
WC3=89 opt{ 15 to 110 }
WC4=89 opt{ 15 to 110 }
LC1=400 opt{ 250 to 1000 }
LC2=400 opt{ 250 to 1000 }
LC3=400 opt{ 250 to 1000 }
LC4=400 opt{ 250 to 1000 }
Delay=-0.4 opt{ -.6 to 0 }
Gain=28 opt{ 0 to 31 }

```

Fig. 5. Variable list for the equalizer components

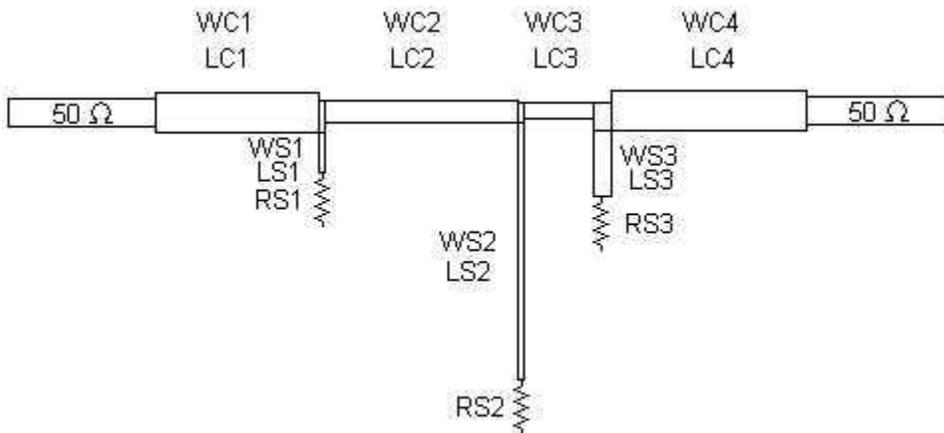


Fig. 6. Variables of the 3 stub equalizer

The schematic is simulated with 15 iterations of the optimizer in gradient mode. The value of each variable must be updated after each simulation. To see the results of the optimization, the NOMINAL OPTIMIZATION element must be removed, or POPPED from the schematic. With the NOMINAL OPTIMIZATION element out of the schematic, the circuit is re-simulated with the updated variables. This process is repeated until an acceptable solution is found. While the process is being repeated, changes to certain variables can be made to see what effect it has on the optimizer converging to a

Var	Eqn	VAR
		VAR1
		WS1=12
		WS2=10
		WS3=63
		LS1=100
		LS2=532
		LS3=258
		RS1=18
		RS2=1500
		RS3=390
		WC1=110
		WC2=60
		WC3=48
		WC4=110
		LC1=490
		LC2=664
		LC3=250
		LC4=555
		Delay=-0.3378
		Gain=31

Fig. 9. Variable list of the final equalizer

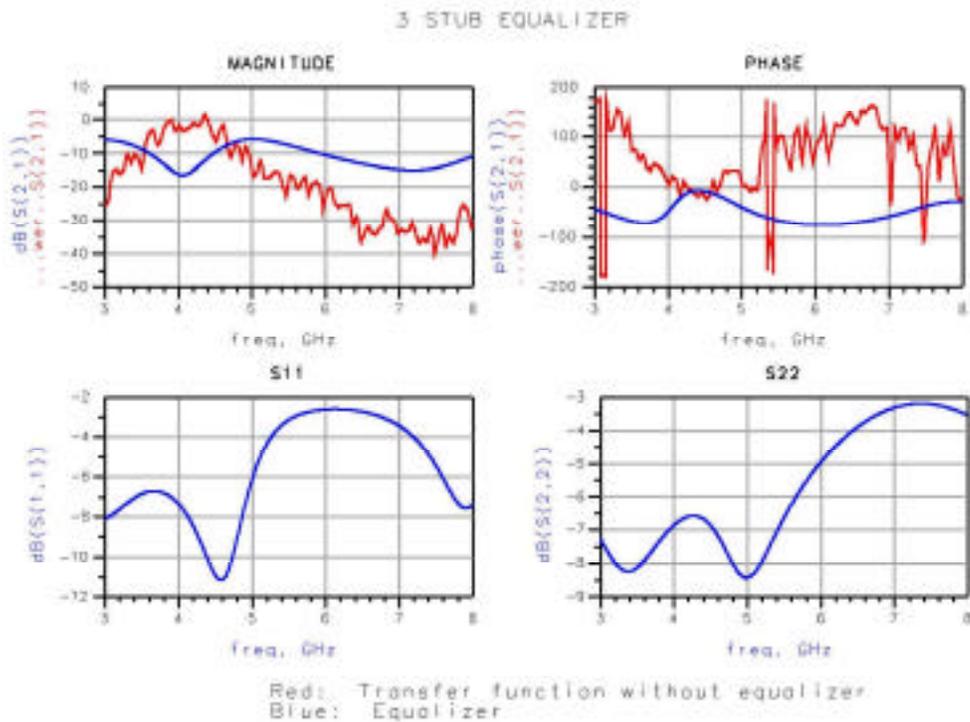


Fig. 10. Simulated results of the final equalizer.

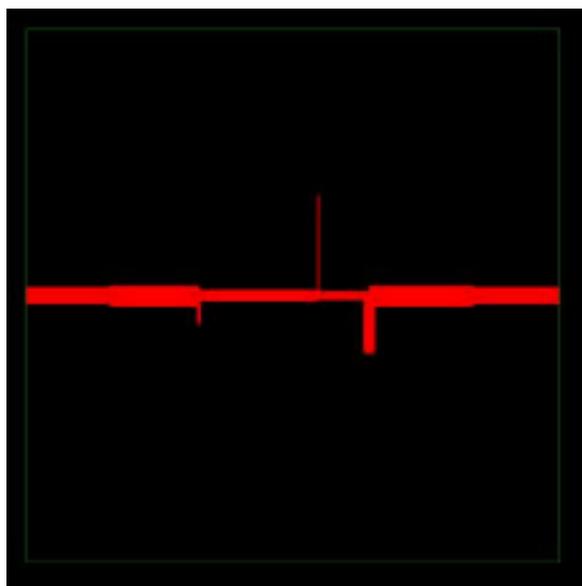


Fig. 11. Layout of the equalizer.

Fabrication of the Equalizer

The equalizer is fabricated on Arlon 31 mil, 2.33 dielectric material. The circuit is etched onto the material using a circuit board etching machine. A photograph of the equalizer is shown in fig 12. Chip resistors are soldered from the end of the stubs to ground. This is done by drilling a hole through the board at the end of the stub. A small piece of copper tape is soldered to the ground plane to cover the hole, and provide a position to solder the resistor to ground. A diagram of how the chip resistor is soldered to ground is shown in fig 13.

A few modifications were made to the equalizer to achieve the desired results. The length of each stub had to be shortened, and a higher value of resistance was used on one of the stubs. The length of each stub was shortened to compensate for the length of each chip resistor, which was not accounted for in simulations. Stub 1 was shortened from 100 mils to 90 mils, stub 2 was shortened from 523 mils to 408 mils, and stub 3 was shortened from 258 mils to 228 mils. The value of resistance had to be increased because the depth of the notch at 4.1 GHz was only -13 dB. The resistor on stub 2 was increased from 1.5 kOhms to 1.8 kOhms. The increase in resistor value increased the depth of the notch at 4.1 GHz to -15 dB. The measured results versus the simulated results are shown in fig 14. The total length of the equalizer is 412 ps. The measured return loss does not match the simulated results exactly, but the return loss is still better than -6 dB across the band.

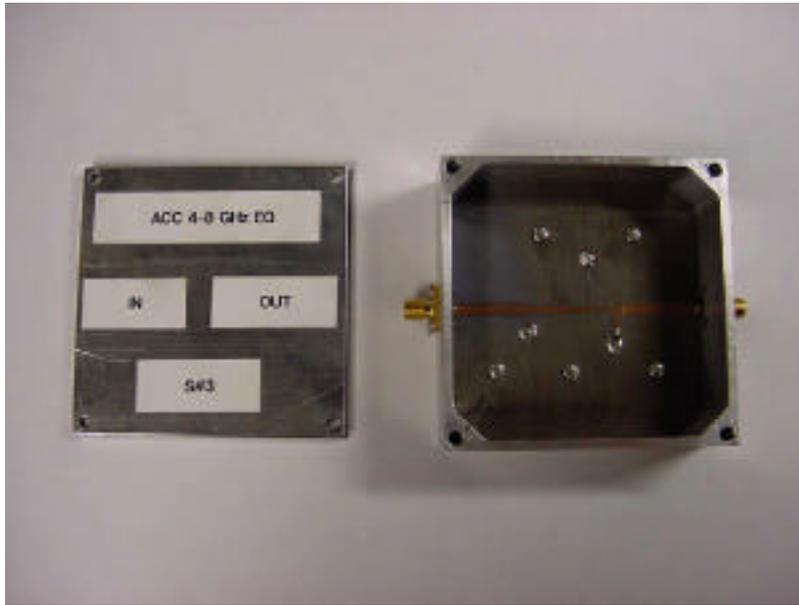


Fig. 12. Photograph of the equalizer

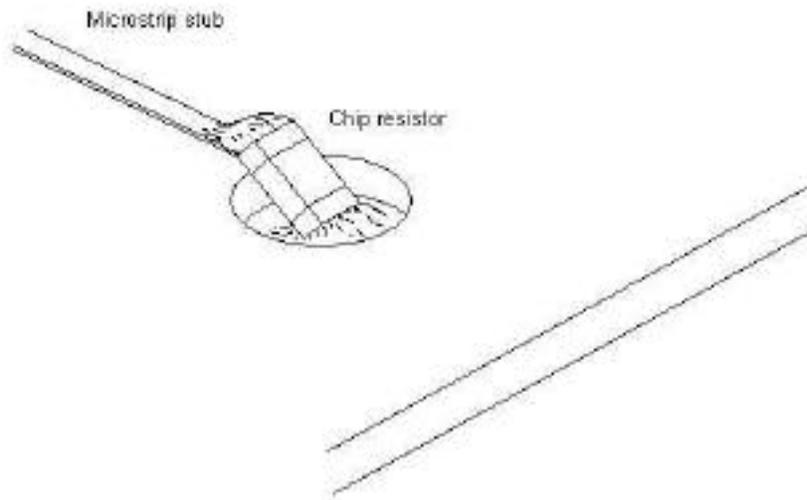


Fig. 13. Diagram of the soldered chip resistor

4-8 GHz ACCUMULATOR EQUALIZER

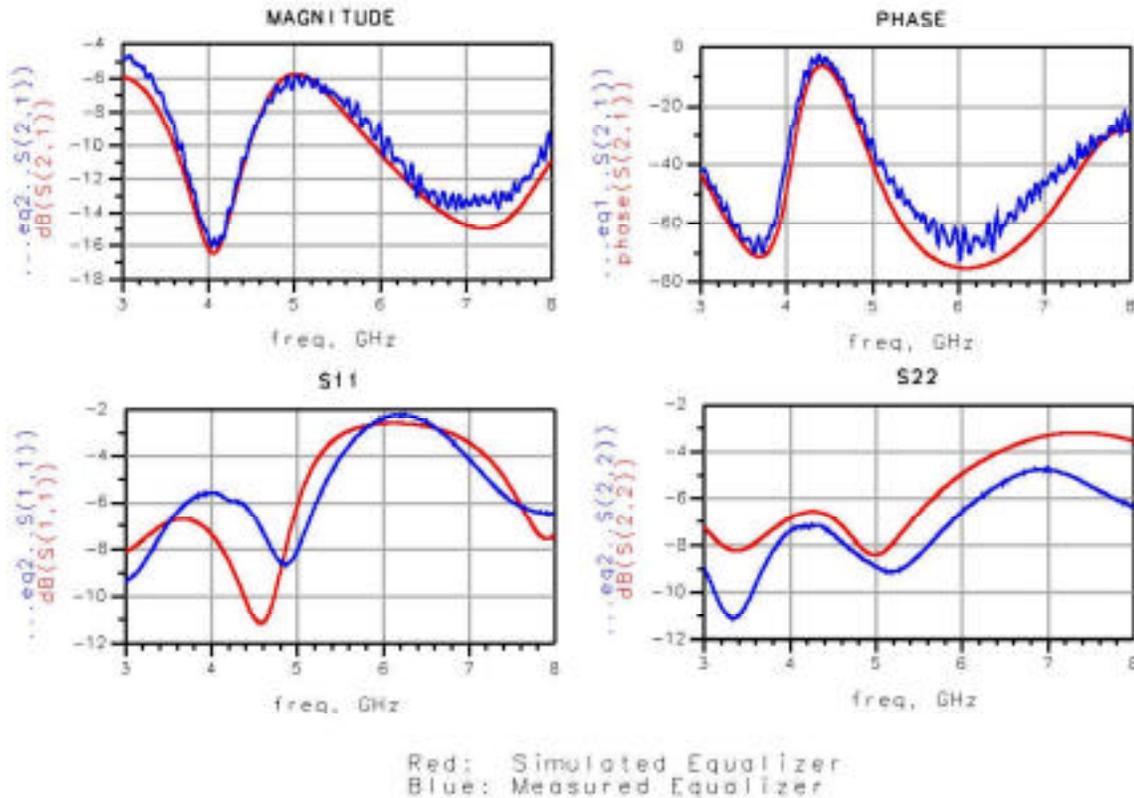


Fig. 14. Measured versus simulated results of the equalizer

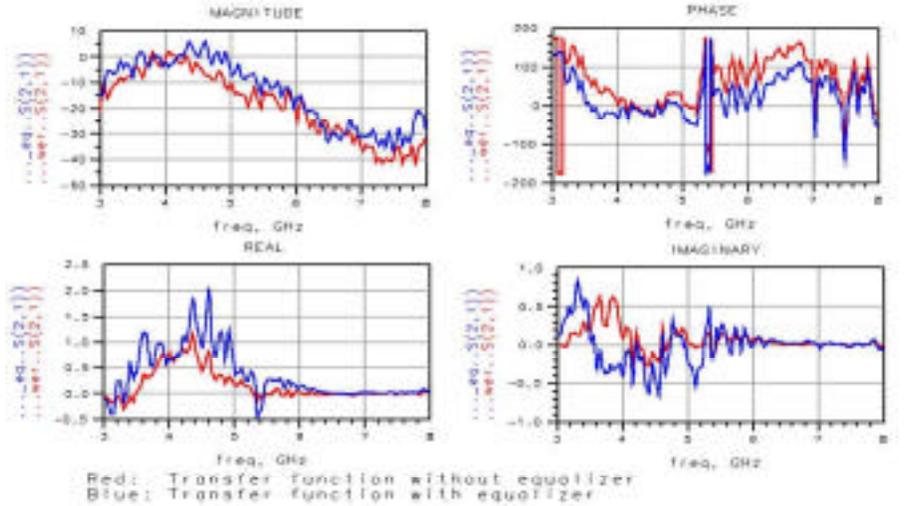
A figure of merit for the equalizer is the integrated real part. The integrated real part is the part of the signal that does the cooling for the system. The integrated negative real part actually does the cooling, but since a 180 degree phase shift is added to the measurements here, the integrated positive real part is calculated. Fig 15 shows the integrated real part of the transfer function. The integrated real part is $7.905e8$ for the system without the equalizer, and the integrated real part is $1.7934e9$ with the equalizer. This shows the system is improved by more than a factor of 2.

The equalizers were mounted on the low level plate in the AP 10 stub room. There is one equalizer for the horizontal system and one equalizer for the vertical system. A photograph of the equalizers on the plate is shown in fig 16.

4 - 8 GHz ACCUMULATOR SYSTEM

Transfer function of the system with and without the measured equalizer data

The integrated real part is calculated in the bottom right corner



Red: Transfer function without equalizer
Blue: Transfer function with equalizer

INTEGRATED REAL PART

Without equalizer	With equalizer
noeq	witheq
7.90528	1.79429

```

>>> noeq=integrate(real(hor_lower.S(2,1)))
>>> witheq=integrate(real(hor_low_w_eq.S(2,1)))
    
```

Fig. 15. Integrated real part of the accumulator system

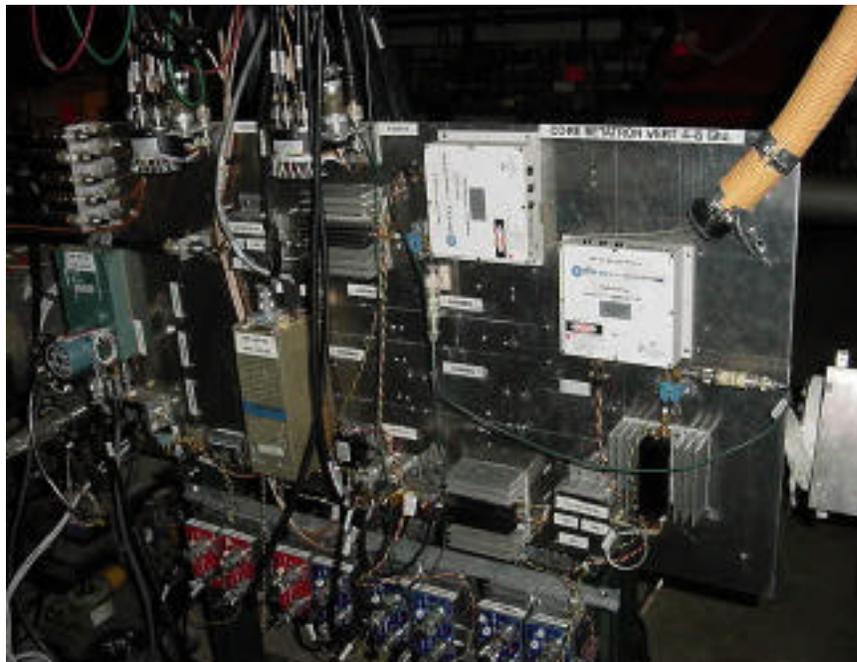


Fig. 16. Photograph of the equalizers mounted in the AP 10 stub room