

# A Multi-Batch Fast Bunch Integrator for the Fermilab Main Ring

G. Vogel, B. Fellenz and J. Utterback

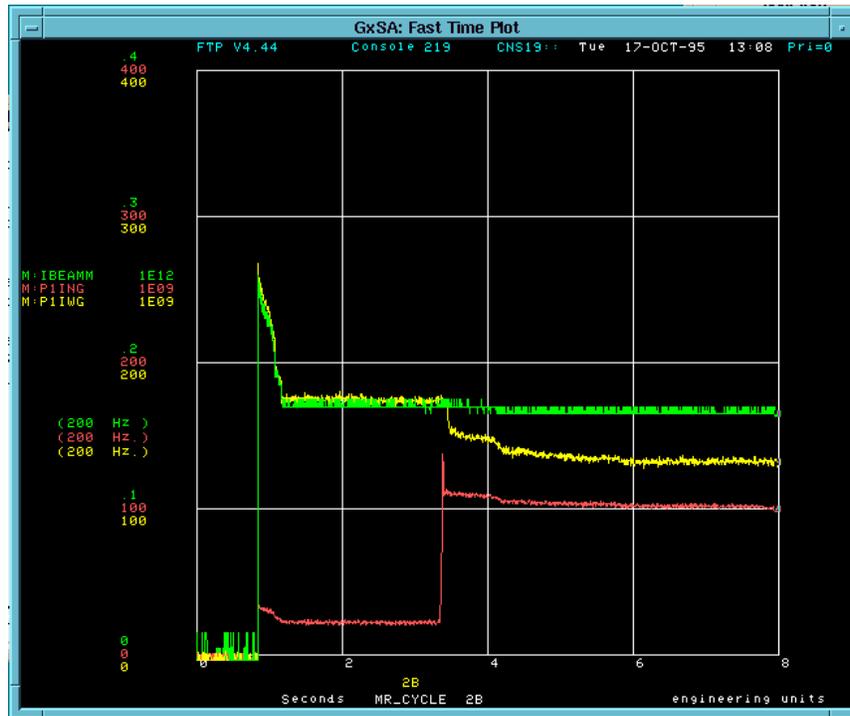
*Fermi National Accelerator Laboratory  
P.O. Box 500, Batavia, IL 60510*

**Abstract.** In order to support new multi-batch coalescing scenarios in the Fermilab Main Ring and Main Injector a new Fast Bunch Integrator system has been developed and installed. This VME based system provides the capability to measure both the batch and central bunch intensities for up to 12 proton or 4 antiproton batches at a time in the accelerator. The system provides for variable batch lengths of up to 15 bunches and central bunch spacing down to 21 RF buckets (394 nanoseconds). A new dual channel fast integrator circuit has been designed for the system which attains 50 dB of dynamic range with programmable integration windows to 18.8 nanoseconds in length with 2 nanosecond rise/fall times.

## INTRODUCTION

One of the many ways used to achieve higher luminosity operations in colliding beam physics is to use higher intensity bunches for the collisions. One of the ways this is accomplished at Fermilab is to take a group of bunches (batch) and, through a process of RF manipulation known as coalescing, converting them into a single bunch containing the majority of their previous intensity. This process is presently carried out in the Main Ring.

In order to determine the efficiency of this process and monitor where losses occur during it, a real time intensity measuring system known as a Fast Bunch Integrator (FBI) was developed. Utilizing a signal from the Main Ring Resistive Wall Current Monitor this system was able to measure the intensity of both the original batch and its central bunch by using both wide gated and narrow gated integrators. A comparison of these two measurements after coalescing provides a measure of the coalescing efficiency. The original FBI system was capable of measurements on a single batch.



**Figure 1.** FBI Plot of Single Bunch Coalescing

As another way of increasing luminosity the Tevatron is moving to operations using more coalesced bunches (36 on 36 vs. 6 on 6). To accomplish this, multiple batches will be coalesced in the Main Ring simultaneously for injection into the Tevatron. This multi-batch operation involves coalescing up to 12 proton or 4 antiproton (pbar) batches at one time. In support of the new multi-batch operations a new Main Ring FBI has been developed. The new FBI system supports fast time plots, snapshot plots and datalogging of bunch intensity for all bunches as well as providing sums of bunch intensities (for use as transfer qualifiers) for both wide and narrow integration gates. The narrow gates provide the integrated intensity for individual bunches (P1-P12, A1-A4) while the wide gates provide the integrated intensity for an adjustable sized batch centered on each narrow gated bunch. The system has been scaled for a maximum bunch intensity of  $400E9$  particles per bunch. The new FBI is a VME based system utilizing a Motorola MVME-162LX embedded computer. It has been designed to provide sufficient functional flexibility to be used in the main injector with minimal software modification (only that required to adopt the gating for a machine with a different harmonic number). A typical fast time plot of coalescing studies using the new FBI system is shown in figure 1. Beam is seen entering the machine at approximately 1 S with the lower trace being that beam in the central bunch. The beam is accelerated up to 150 GeV with some losses and at about 3 S

coalescing takes place. In this case not all the beam has been recaptured in the central bunch as is seen by the difference between the wide (M:PIIWG) and narrow (M:PIING) gate plots.

## SYSTEM HARDWARE

The system is VME based using an embedded controller with an ethernet interface to the accelerator control system. The hardware consists of a timer board (VRFT), a Tevatron clock decoder (VUCD), two digitizers (Omnibyte Comet) and two gated integrator modules along with the embedded processor (Motorola MVME-162LX) in a modified Tracewell VME chassis. A block diagram of the system is shown in figure 2. While most of the system hardware is either commercial or Fermilab AD/Controls general purpose modules, the dual channel gated integrator modules were specifically designed for this project. This was due to the high speed requirements of the analog processing. The integrator circuit needed to be capable of being gated with integrate windows as short as 18.8 nS with 2 nS maximum rise and fall times, cleared with reset pulses of 50 nS and be ready to integrate again all within 384 nS. This module is described below.

The Resistive Wall Current Monitor is a wideband (2 GHz), AC coupled, low impedance ( .16 ohms) beam current detector. A full description of these types of detectors can be found in reference 1.

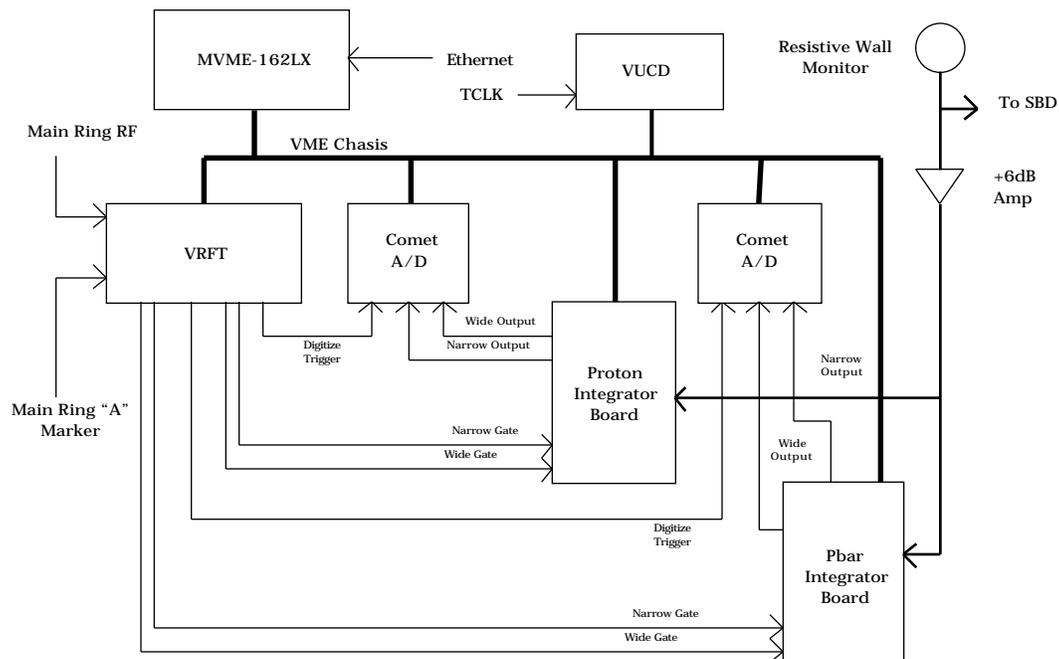


FIGURE 2. Main Ring FBI Block Diagram

The Motorola MVME-162LX is a standard configuration 68040 based single board VME computer. It serves as the system network (ACNET) interface via its ethernet connection and as the VME bus master. It is configured with VxWorks (Wind River Systems) as its operating system. Software programming is performed in "C" and is downloaded via the network. The MVME-162 has 4 MByte of DRAM and 128K of battery backed RAM which is used to store system settings.

The VUCD and VRFT are standard AD/Controls VME clock decoder boards. The VUCD provides Tevatron clock decoding in order to support plotting and datalogging while the VRFT uses Main Ring RF (53 MHz) and a beam sync marker to generate the system data acquisition gates.

The Omnibyte Comet VME A/D board is a 12 bit, 5MS/s VME digitizer with 64 Kword/channel of memory depth and an external trigger. Two channels (0,1) on each board are used to sample the wide and narrow gate integrated intensities based on an external trigger.

## Dual High Speed Integrator

The dual high speed integrator board (figure 3) is a two channel fast gated integrator circuit in a 6U VME form factor. The channels can be configured with jumpers to be either fully independent or have common signal or common trigger

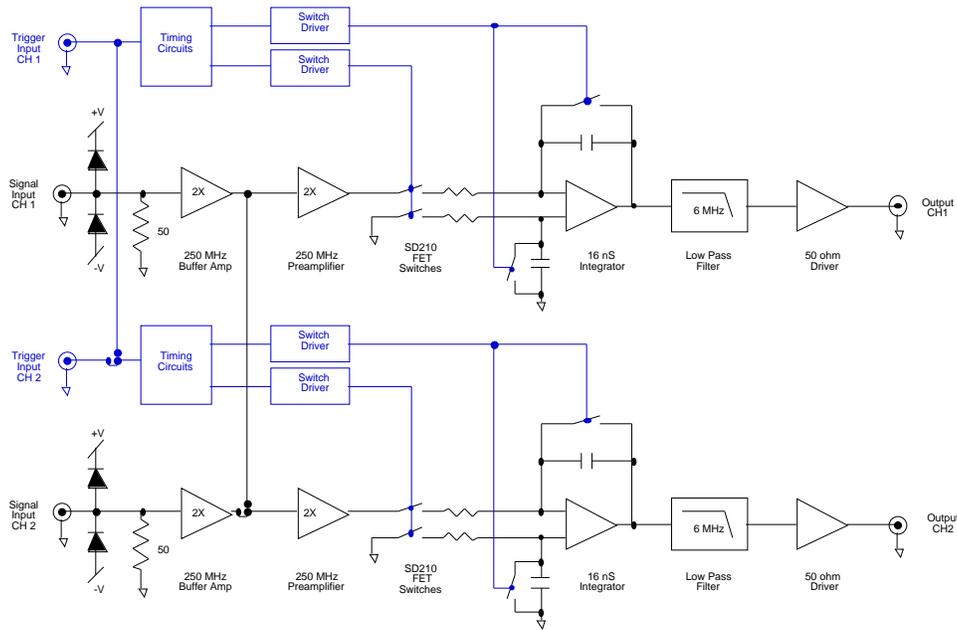
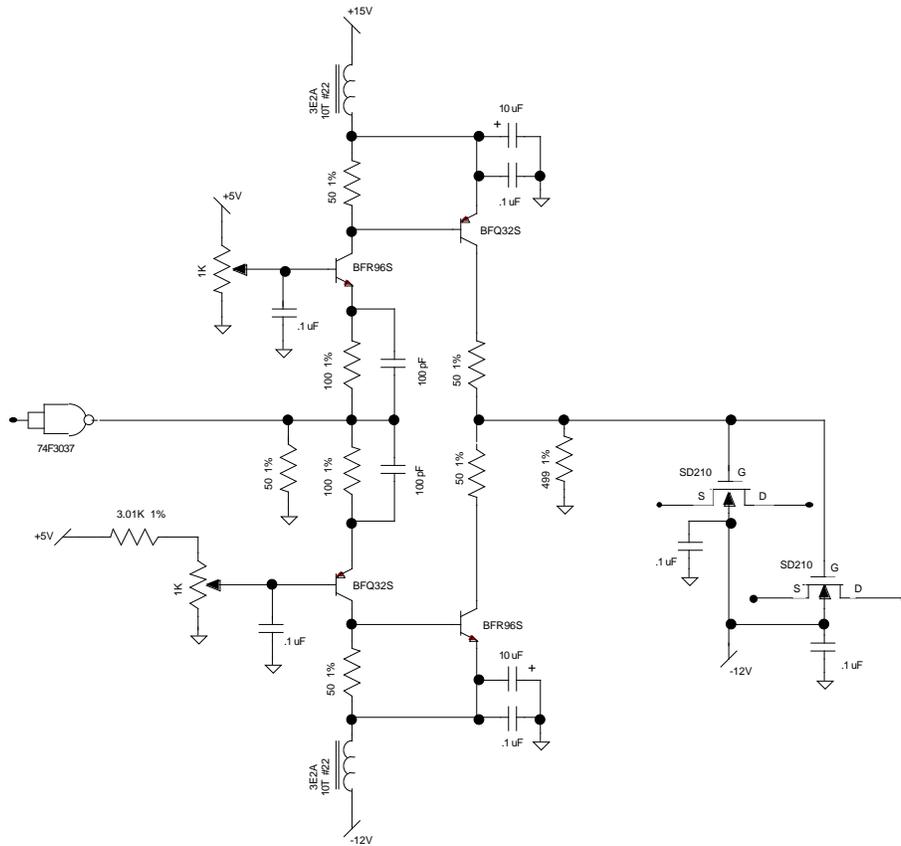


FIGURE 3. Integrator Board Block Diagram



**FIGURE 4. FBI Switch Driver Schematic**

inputs. For the FBI each board is configured for a common input but independent gates for the two integrator channels. The gate width is fixed in hardware at 18.8 nS for the first channel (via jumper) but uses the trigger gate width, controllable from a parameter page, for the second. To accomplish the high speed switching required for the 18.8 nS gates, Siliconix SD210 DMOS FET switches were selected and fast bipolar drivers (figure 4) were designed. The one volt full scale output corresponds to 400E9 particles.

The measured RMS noise level at the output is 1.9 mV, or .19% of full scale and is consistent with the noise specification for the AD843 amplifier used to form the integrator. The 1/f noise below 2 KHz provides the dominant component. This part was selected for its low noise, 34 MHz bandwidth, and small bias current by virtue of the FET input. The buffer amplifier used to optimize the signal level at the integrator switch, has 250 MHz of bandwidth but contributes little noise. Linearity was measured as a function of both input pulse amplitude and width. In both cases, the errors were dominated by the .19% of full

scale RMS noise. The rise and fall time of the switches provide  $\pm 0.5\%$  amplitude accuracy through a 15 nS window for the 18.8 nS wide gate.

Because the resistive wall monitor used for the FBI is AC coupled, the baseline varies depending on bunch intensities and spacing. With 12 bunches spaced by 21 RF buckets, the baseline is estimated to change by  $\pm 0.1\%$  between turns. To correct for this, and remove constant integrator errors, the baseline is measured every other turn and subtracted from the measured intensities in software. The accuracy of this procedure depends on the distribution of bunches and where the baseline is sampled.

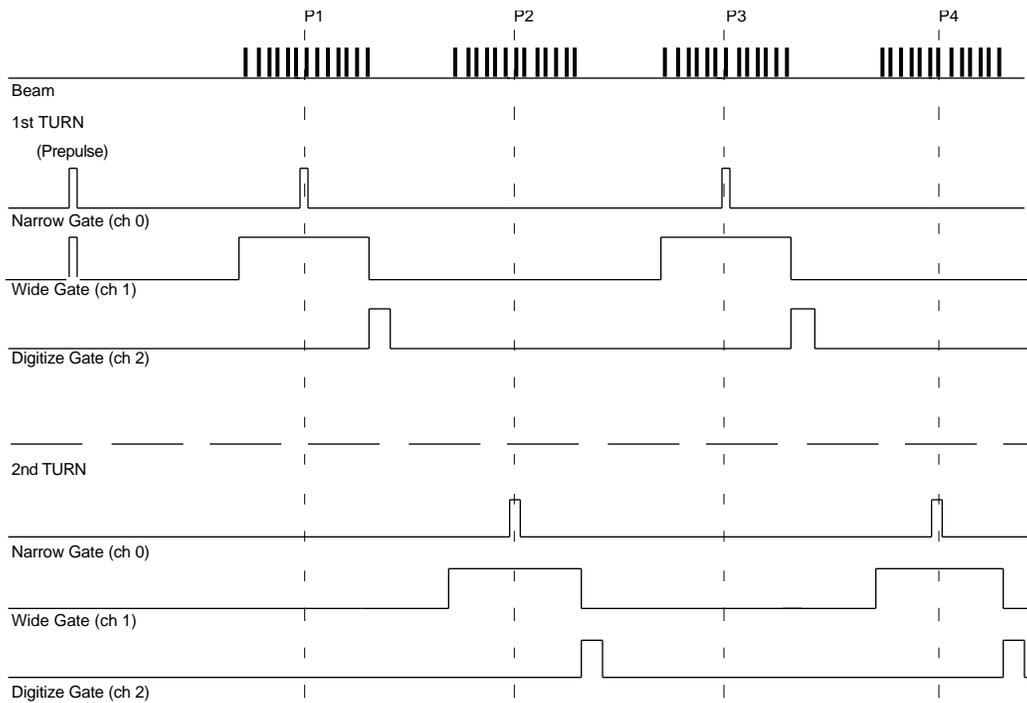
## **SYSTEM SOFTWARE**

The system software is a compiled C program running in the VxWorks operating system of the embedded processor. It performs all data handling, reading the digitizers, sorting data and performing the proton and pbar summations. Data display is provided via standard control system Fast Time and Snapshot Plots, parameter pages or a local terminal.

### **Embedded Processor Application**

A compiled C program running on the embedded processor performs high speed data transfer across the VME back plane along with sorting and summing of the transferred data. The system reads a complete data set when a data request has been issued. The integrated intensities of the 12 proton bunches are digitized by the proton Comet board as gated externally by the VRFT. The intensity data is interleaved (P1-P11 odd, P2-P12 even) in the digitizer FIFO memory. Channel 0 carries the narrow gate data while channel 1 holds the wide gate data. The integrated intensity data for the 4 pbar bunches reside similarly in the pbar digitizer. This data is read out and sorted and used to calculate narrow and wide gate sums for protons and pbars. It then returns only those bunch intensities or sums that have been requested.

When a change of VRFT settings is initiated by a console page, data acquisition stops, the VRFT is disabled, the new memory pattern is configured and downloaded to the VRFT and it is re-enabled. The pattern is triggered on receipt of a request from ACNET or a local terminal and plays over two turns. The pattern is configured with an integrator prepulse (to clear any integrator drift since the last measurement) and odd bunch gates on the first turn followed by even bunch gates and background sample on the second. A partial sample of the gating scheme for protons is shown in figure 5.



**FIGURE 5.** FBI system timing for bunches P1-P4

## Console Control

The ability to change the 12 proton gate delays, the 4 pbar gate delays, the proton and pbar zero sample times, as well as the proton and pbar wide gate widths is provided via a console page application. Bunch delay timing for the system is controlled via the D/A setting of the narrow gate intensity parameter for each bunch and zero sample. This setting is defined in RF buckets. Default bunch spacing is 21 buckets. The standard wide gate setting for protons and pbars is 13 buckets. As each setting is changed it is sent to the local processor for use in reconfiguring the VRFT. Data can be displayed using standard console plotting packages (fast time plot and snapshot plot) as well as by monitoring the parameter page. Fast time plot rates of up to 720 Hz are supported and a maximum sample rate of 23KHz is available on the snapshot plots.

## CONCLUSIONS

The system has been in operational use in the Fermilab Main Ring since October 1995. It has provided all the Main Ring FBI data for both the 36 on 36 operation studies and the last months of Collider Run Ib. It has proven a reliable,

easy to use and easy to maintain system for real time individual bunch intensity monitoring.

## **ACKNOWLEDGEMENTS**

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## **REFERENCES**

1. Webber, R.C., "Longitudinal Emittance: An Introduction to the Concept and Survey of Measurement Techniques Including Design of a Wall Current Monitor," AIP Conference Proceedings No.212, pp. 85-126.
2. Utterback, J., and Vogel, G., "Fast Bunch Integrator, A System for Measuring Bunch Intensities in Fermilab's Main Ring," presented at ICALEPCS 95, Chicago, IL, October 29,1995.
3. Wang, X., "Ultrafast, High Precision Gated Integrator," AIP Conference Proceedings No.333, 1994, pp. 260-266.